DDR I/II Termination Regulator

FEATURES

- Operation Supply Voltage: 1.6V to 5.5V
- Low Supply Current: 207μA @ 2.5V
- Low Output Offset
- Source and Sink Current
- Low External Component Count
- No Inductor Required
- No external Resistors Required
- Thermal Shutdown Protection
- Suspend to RAM (STR) Function
- PSOP-8 with Power-Pad Package

TYPICAL APPLICATIONS

- DDR-SDRAM Termination Voltage
- DDR-I / DDR-II Termination Voltage
- SSTL-2
- SSTL-3

DESCRIPTION

The FT550 is a linear regulator designed to meet the JEDEC SSTL-18, SSTL-2 and SSTL-3 (Series Stub Termination Logic) specifications for termination of DDR-SDRAM. It contains a high-speed operational amplifier that provides excellent response to the load transients. This device can deliver 1.5A/0.9A continuous current and transient peaks up to 3A/1.8A in the application as required for DDRI/II-SDRAM termination. With an independent VS pin, the FT550 can provide superior load regulation. The FT550 provides a VREF output as the reference for the applications of the chipset and DIMMs.

The FT550 can easily provide the accurate VTT and VREF voltages without external resistors that PCB areas can be reduced. The quiescent current is as low as 207μA @ 2.5V. So the power consumption can meet the low power consumption applications.

The FT550 also has an active high enable pin (EN) that provides Suspend to RAM (STR) functionality. When EN is pulled low, the VTT output will be tri-state providing a high impendence, but VREF will remain active. A power saving advantage can be obtained in this mode through lowering the quiescent current to 153μA @ 2.5V.

TYPICAL APPLICATION CIRCUIT

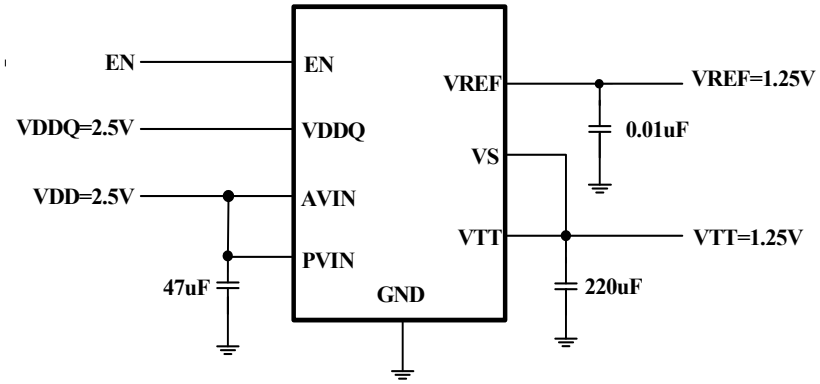


Figure 1: Typical Application Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage

PVIN, AVIN, VDDQ to GND.....-0.3V to +6V

Operating Ambient Temperature Range, T_A.....-40°C to +85°C

Maximum Junction Temperature, T_J.....150°C

Storage Temperature Range, T_{STG}.....-65°C to+150°C

Reflow Temperature (soldering, 10 sec).....260°C

Electrostatic Discharge, V_{ESD}

Human body mode.....2000V

Machine mode.....200V

Thermal Resistance Junction to Ambient, (θ_{JA})

PSOP-8.....50°C/W

Thermal Resistance Junction to Case, (θ_{JC})

PSOP-8..... 12°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

PIN CONFIGURATION

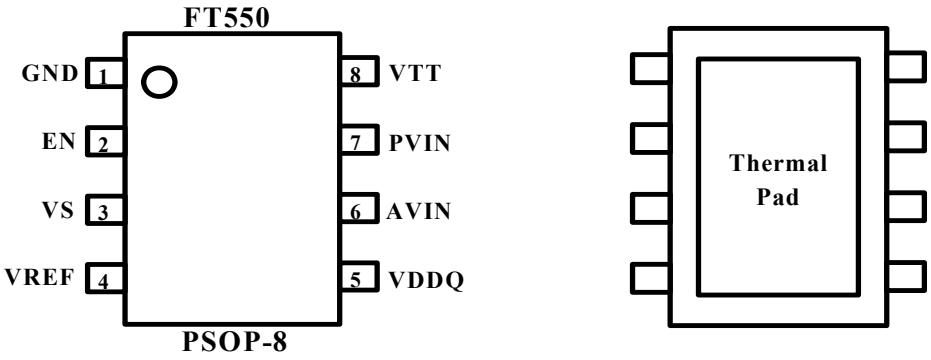


Figure 2: Pin Assignments

TERMINAL DEFINITION

Number	Name	Function
1	GND	Ground
2	EN	Active low shutdown control pin
3	VS	Feedback pin for regulating VTT
4	VREF	Buffered output that is a reference output of VDDQ/2
5	VDDQ	Power Input for internal reference
6	AVIN	Analog input pin
7	PVIN	Power input pin
8	VTT	Output voltage for connection to termination resistors, equal to VDDQ/2

Table 1

ORDERING INFORMATION

Order Num.	Temp. Range	Package
FT550	-40°C to 85°C	PSOP-8

Table 2

MARKING RULE

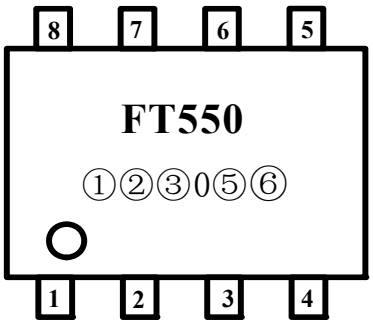


Figure 3: PSOP-8 (Top View)

① Represent Year
② Represent Week
③ Represent Lot
④ Represent Vacant
⑤ Represent Manufactory
⑥ Represent Version

RECOMMEND OPERATION RANGE

Operating Ambient Temperature Range

T_A.....-40°C to +85°C

AVIN to GND.....1.6V to +5.5V

PVIN, EN, VDDQ to GND.....1.6V to AVIN

BLOCK DIAGRAM

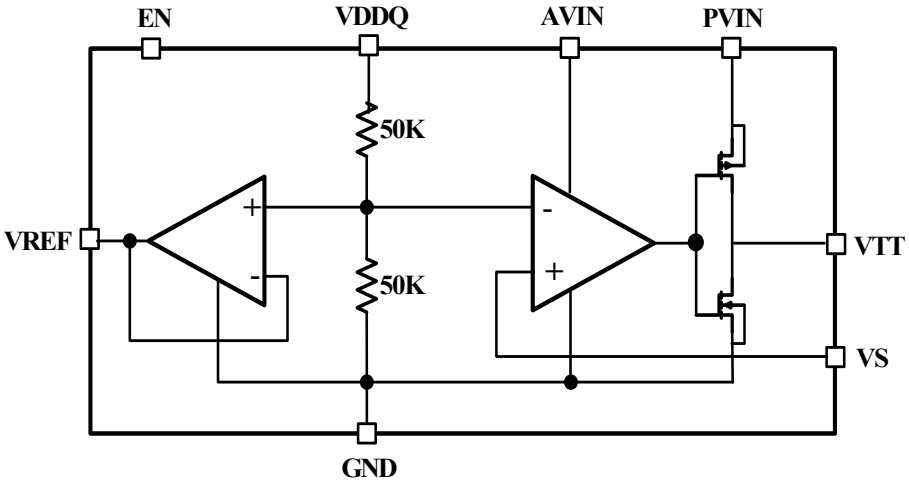


Figure 4: Block Diagram

ELECTRICAL CHARACTERISTICS

Specifications with standard typeface are for TA=25°C,unless otherwise specified, AVIN=PVIN=2.5V, VDDQ=2.5V for DDR I, AVIN=PVIN=VDDQ=1.8V for DDRII.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VREF Voltage	VREF	VDDQ =1.7V	0.81	0.848	0.89	V
		VDDQ =1.8V	0.86	0.899	0.94	V
		VDDQ =1.9V	0.91	0.949	0.99	V
VREF Voltage	VREF	VDDQ =2.3V	1.11	1.150	1.19	V
		VDDQ =2.5V	1.21	1.250	1.29	V
		VDDQ =2.7V	1.31	1.349	1.39	V
VREF Output impendence	Z_{REF}	I_{REF} =-30μA to + 30μA	---	1.15	---	kΩ
VTT Output voltage	VTT	I_{OUT} = 0A				
		VDDQ =1.7V	0.81	0.847	0.89	V
		VDDQ =1.8V	0.86	0.896	0.94	V
		VDDQ =1.9V	0.91	0.947	0.99	V
		I_{OUT} = ±0.9A				
		VDDQ =1.7V	0.81	0.847	0.89	V
		VDDQ =1.8V	0.86	0.896	0.94	V
		VDDQ =1.9V	0.91	0.947	0.99	V
VTT Output voltage	VTT	I_{OUT} = 0A				
		VDDQ =2.3V	1.11	1.152	1.19	V
		VDDQ =2.5V	1.21	1.252	1.29	V
		VDDQ =2.7V	1.31	1.352	1.39	V
		I_{OUT} = ±1.5A				
		VDDQ =2.3V	1.11	1.152	1.19	V
		VDDQ =2.5V	1.21	1.252	1.29	V
		VDDQ =2.7V	1.31	1.352	1.39	V
VTT Output Voltage Offset (VREF- VTT)	VTT_{OS}	I_{OUT} = 0A	-40	0	40	mV
		I_{OUT} = -0.9A	-40	0	40	mV
		I_{OUT} = +0.9A	-40	0	40	mV
VTT Output Voltage Offset (VREF- VTT)	VTT_{OS}	I_{OUT} = 0A	-40	0	40	mV
		I_{OUT} = -1.5A	-40	0	40	mV
		I_{OUT} = +1.5A	-40	0	40	mV

ELECTRICAL CHARACTERISTICS (continues)

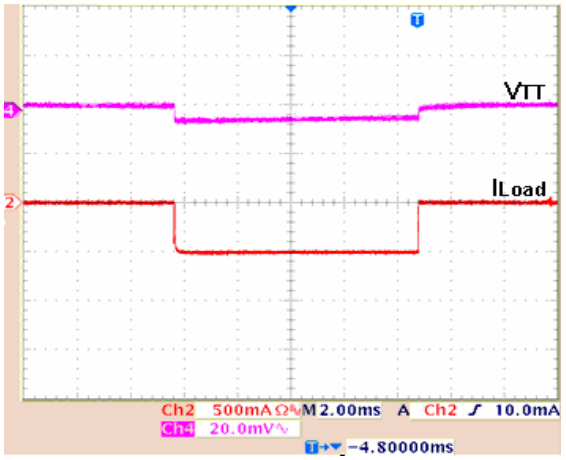
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Quiescent Current	I_Q	I_{OUT} = 0A	---	207	500	μA
VDDQ input Impedance	Z_{VDDQ}		---	100	---	KΩ
Quiescent Current in shutdown	I_{EN}	EN = 0	---	154	270	μA
Shutdown leakage current	I_{Q_EN}		---	0.47	---	μA
VS input current	I_{VS}		---	37	---	pA
VTT leakage current in shutdown	I_V	EN = 0, VTT = 1.25V	---	300	---	pA
Minimum Shutdown High Level	V_{IH}		1.6	---	---	V
Maximum Shutdown Low Level	V_{IL}		---	---	0.8	V
Thermal Shutdown	T_{EN}		---	150	---	°C
Thermal Shutdown Hysteresis	T_{Hsy}		---	25	---	°C

Table 3

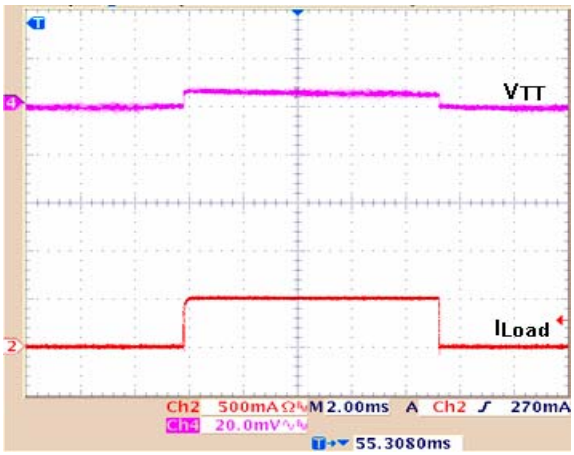
TYPICAL PERFORMANCE CHARACTERISTICS

AVIN=2.5V, PVIN=2.5V, VDDQ=2.5V, C_{AVIN}=0.1µF, C_{PVIN}=47µF, C_{VREF}=0.01µF, EN=2.5V, C_{VTT}=330µF*2/6.3V POSCAP Series/SANYO, T_A=25°C, unless otherwise noted.

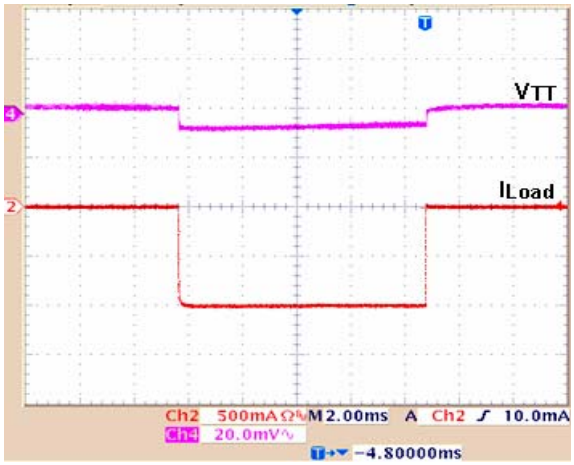
ILoad=0.5A Transient(Sourcing)



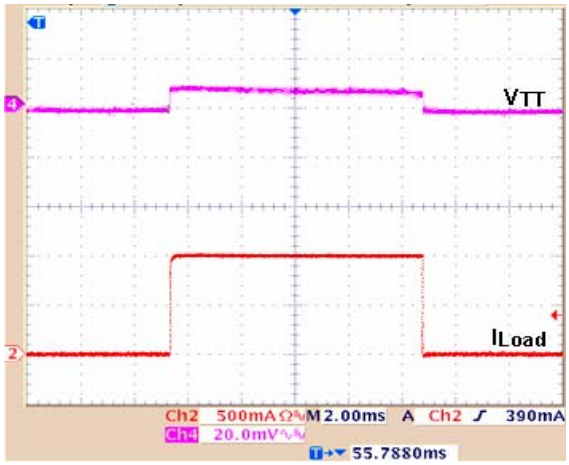
ILoad=0.5A Transient(Sinking)



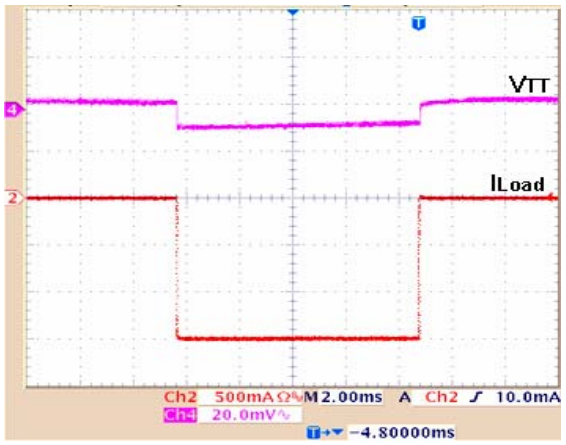
ILoad=1A Transient(Sourcing)



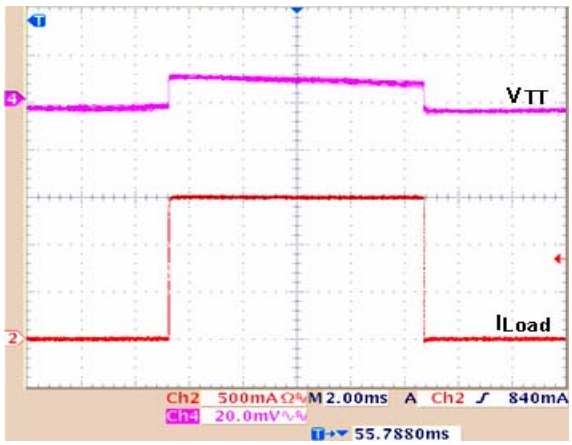
ILoad=1A Transient(Sourcing)



ILoad=1.5A Transient(Sourcing)



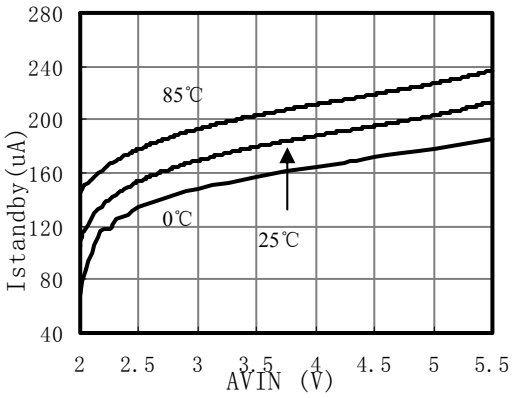
ILoad=1.5A Transient(Sinking)



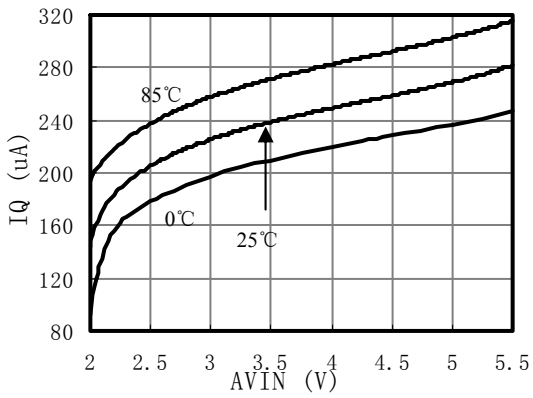
TYPICAL PERFORMANCE CHARACTERISTICS (continues)

AVIN=2.5V, PVIN=2.5V, VDDQ=2.5V, C_{AVIN}=0.1µF, C_{PVIN}=47µF, C_{VREF}=0.01µF, EN=2.5V, C_{VTT}=220µF, T_A=25°C, unless otherwise noted.

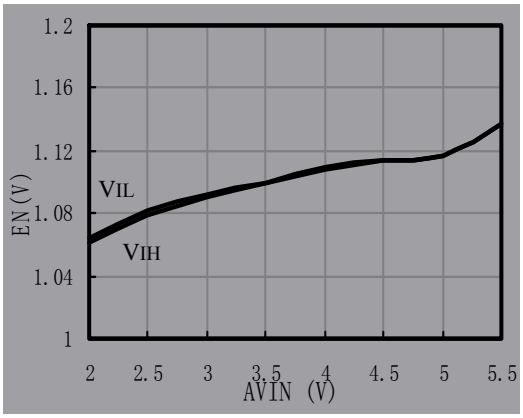
Istandby & AVIN Temperature



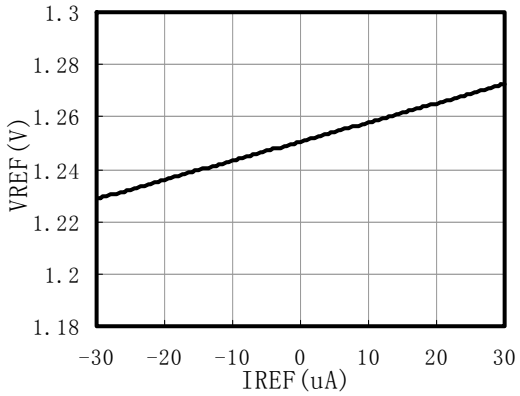
IQ & AVIN Temperature



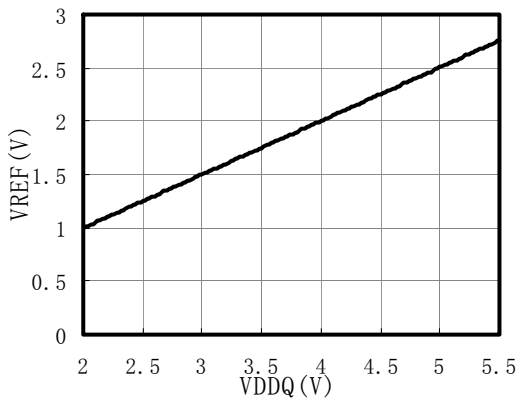
V_{IH} & V_{IL}



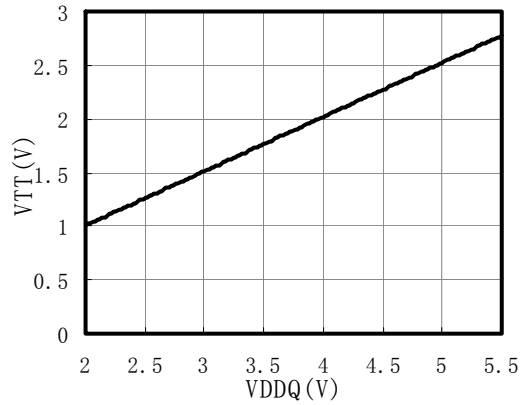
VREF & IREF



VREF & VDDQ



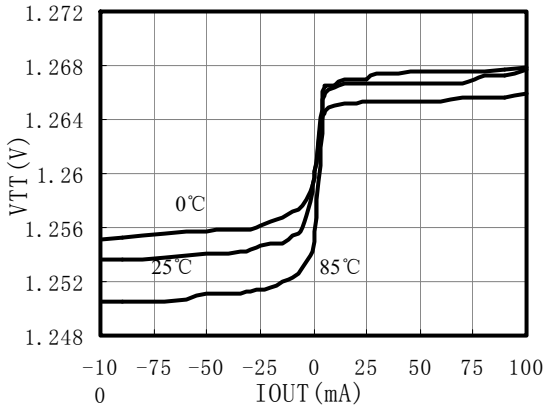
VTT & VDDQ



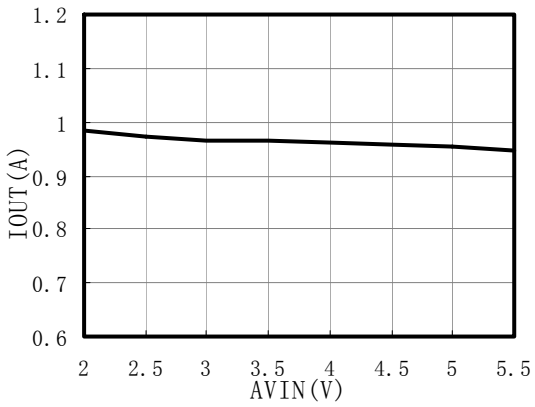
TYPICAL PERFORMANCE CHARACTERISTICS (continues)

AVIN=2.5V, PVIN=2.5V, VDDQ=2.5V, C_{AVIN}=0.1µF, C_{PVIN}=47µF, C_{VREF}=0.01µF, EN=2.5V, C_{VTT}=220µF, T_A=25°C, unless otherwise noted.

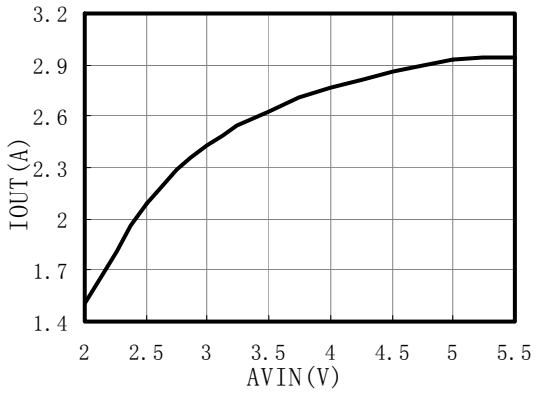
VTT vs IOUT Temperature



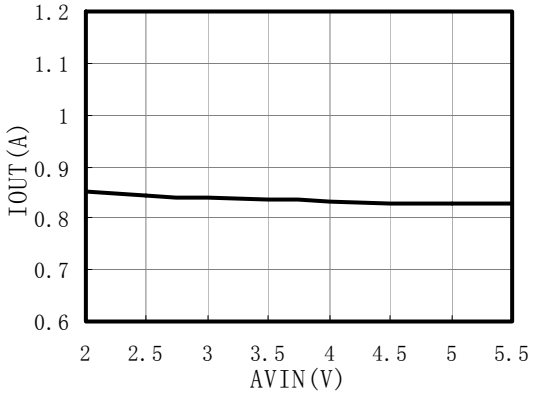
Maximum Sourcing Current vs AVIN (VDDQ=1.8V,PVIN=1.8V)



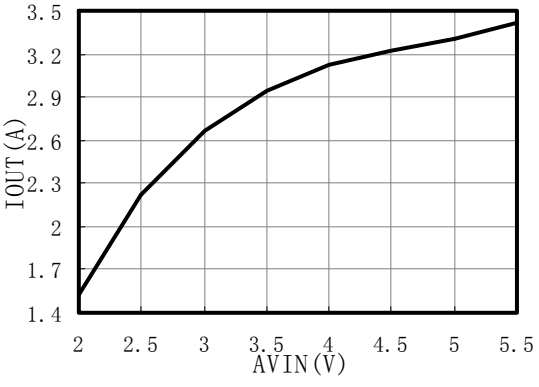
Maximum Sinking Current vs AVIN (VDDQ=1.8V)



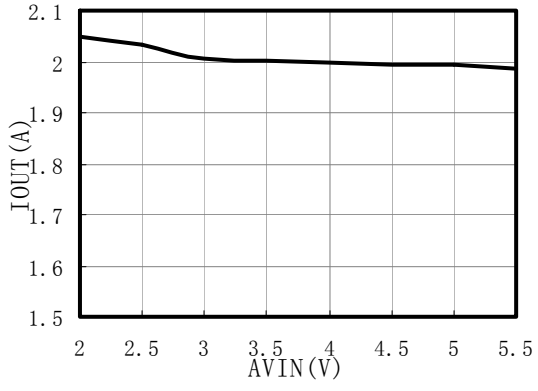
Maximum Sourcing Current vs AVIN (VDDQ=2.5V,PVIN=1.8V)



Maximum Sinking Current vs AVIN (VDDQ=2.5V)



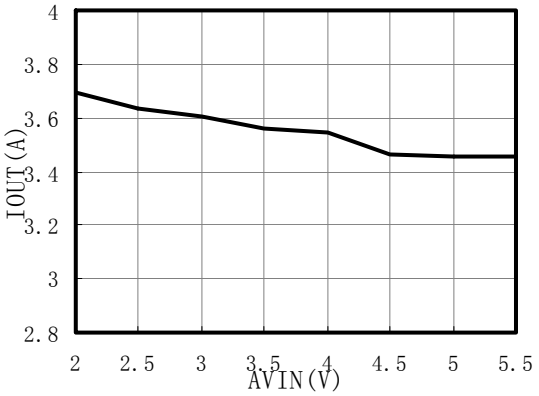
Maximum Sourcing Current vs AVIN (VDDQ=2.5V,PVIN=2.5V)



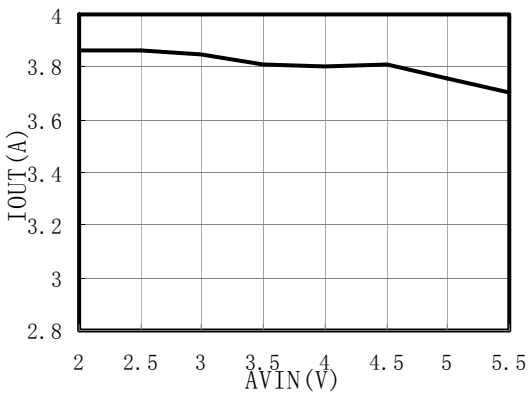
TYPICAL PERFORMANCE CHARACTERISTICS (continues)

AVIN=2.5V, PVIN=2.5V, VDDQ=2.5V, C_{AVIN}=0.1µF, C_{PVIN}=47µF, C_{VREF}=0.01µF, EN=2.5V, C_{VTT}=220µF, T_A=25° C, unless otherwise noted.

Maximum Sourcing Current vs AVIN
(VDDQ=2.5V,PVIN=3.3V)



Maximum Sourcing Current vs AVIN
(VDDQ=1.8V,PVIN=3.3V)



FUNCTIONAL DESCRIPTION

The FT550 is a linear bus termination regulator designed to meet the JEDEC SSTL-2 and STL-3 (Series Stub Termination Logic) specifications for termination of DDR-SDRAM. The output, VTT, is capable of sinking and sourcing current while regulating the output voltage equal to VDDQ/2. The FT550 is designed to maintain the excellent load regulation and with fast response time to minimum the transition preventing shoot-through. The FT550 also incorporates two distinct power rails that separate the analog circuitry (AVIN) from the power output stage (PVIN). This Power rails split can be utilized to reduce the internal power dissipation. And this also permits FT550 to provide a termination solution for the next generation of DDR-SDRAM (DDR II).

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one RS series resistor from the chipset to the memory and one RT termination resistor, both 25Ω typically. The resistors can be changed to scale the current requirements from the FT550. This implementation can be seen below in Figure 5.

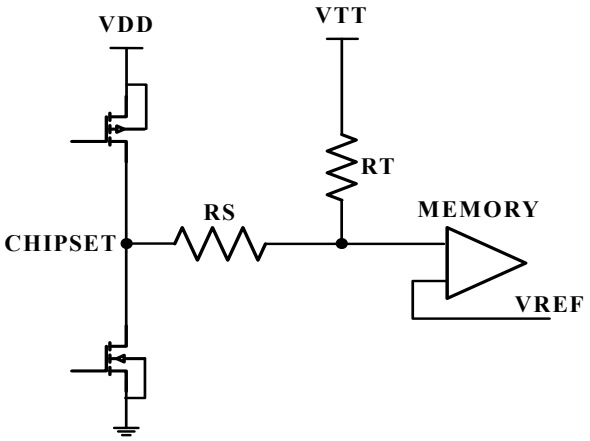


Figure 5: SSTL-Termination Scheme

1. AVIN, PVIN

AVIN and PVIN are two independent input supply pins for the FT550. AVIN is used to supply all the internal analog circuits. PVIN is only used to supply the output stage to create the regulated VTT. To keep the regulation successfully, AVIN should be equal to or larger than PVIN. Using a higher PVIN voltage will produce a larger sourcing capability from VTT. But the internal power loss will also increase and then the heat increases. If the junction temperature exceeds the thermal shutdown threshold than the FT550 will enter the shutdown state that is the same as manual shutdown, where VTT is tri-state and VREF remains active. For SSTL-2 applications, the AVIN and PVIN can be short together at 2.5V to minimize the PCB complexity and to reduce the bypassing capacitors for the two supply pins separately.

2. VDDQ

A voltage divider of two 50kΩ is connected between VDDQ and ground, to create the internal reference voltage (VDDQ/2). This guarantees that VTT will track VDDQ/2 precisely. The optimal implementation of VDDQ is as a remote sensing. This can be achieved by connecting VDDQ directly to the 2.5V rail (SSTL-2 applications) at the DIMM instead of AVIN and PVIN. This will ensure that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines.

3. VS

The VS pin is the feedback sensing pin of the operation amplifier which regulates the VTT voltage. In most motherboard applications, the termination resistors will connect VTT in a long plane. If using the remote sensing pin – VS to the middle of the bus, the significant long-trace IR drop resulting in a termination voltage which is lower at one end than the other can be avoided. This will provide a better distribution across the entire termination bus. If the remote load regulation is not used, the VS pin must still be connected to VTT for correct regulation. Care should be taken when a long VS trace is implemented in close proximity to the memory. Noise pickup in the VS trace can cause problems with precise regulation of VTT. A small 0.1μF ceramic capacitor placed next to the VS pin can help to filter any high frequency signals and preventing errors.

4. VREF

VREF provides a buffered output of the internal reference voltage (VDDQ/2). It can support the reference voltage of Northbridge chipset and memory. This output remains active during the shutdown state and thermal shutdown events to support the suspend to RAM (STR) functionality. For better performance, using an output bypass capacitor close this pin is more helpful for the noise. A ceramic capacitor in the range of 0.1μF to 0.01μF is recommended.

5. VTT

VTT is the regulated output that is used to terminate the bus resistors of DDR-SDRAM. It can precisely track the VDDQ/2 voltage with the sinking and sourcing current capability. The FT550 is designed to deliver 1.5A continuous current and peak current up to 3A with a fast transient response at 2.5V supply rail. The maximum continuous current sourcing from VTT is a function of PVIN. Using a higher PVIN will increase the source current from VTT, but it also increase the internal power dissipation and reduce the efficiency. Although the FT550 can deliver the larger current, care should be taken for the thermal dissipation when larger current is required. The FT550 is packaged with Power-Pad to increase the power dissipation capability. When driving larger current, the larger heat-sink in the PCB is strongly recommended to have a better thermal performance. The R_{DS} of MOS will increase when the junction temperature increases. If the heat is not handled well, the maximum output current will be degraded. When the temperature exceeds the junction temperature, the thermal shutdown protection is activated. That will drive the VTT output into tri-state until the temperature returns below the hysteretic trigger point.

6. Capacitors

The FT550 does not require the capacitors for input stability, but it is recommended for improving the performance during large load transition to prevent the input power rail from dropping, especially for PVIN. The input capacitor for PVIN should be as close as possible. The typical recommended value is 50μF for AL electrolytic capacitors, 10μF with X5R for the ceramic capacitors. To prevent the excessive noise coupling into this device, an additional 0.1μF ceramic capacitor can be placed on the AVIN power rail for the better performance. The output capacitor of the FT550 is suggested to use the capacitors with low ESR. Using the capacitors with low ESR (as ceramic, OS-CON, tantalum) will have the better transition performance which is with smaller voltage drop when the peak current occurring at the transition. As a general recommendation the output capacitor should be sized above 220μF with the low ESR for SSTL applications with DDR-SDRAM.

7. Thermal Dissipation

When the current is sinking to or sourcing from VTT, the FT550 will generate internal power dissipation resulting in the heat. Care should be taken to prevent the device from damages caused by the junction temperature exceeding the maximum rating. The maximum allowable internal temperature rise (T_{RMAX}) can be calculated under the given maximum ambient temperature (T_{AMAX}) of the application and the maximum allowable junction temperature (T_{JMAX}):

$$T_{RMAX} = T_{JMAX} - T_{AMAX}$$

From this equation, the maximum power dissipation (P_{DMAX}) of the FT550 can be calculated:

$$P_{DMAX} = T_{RMAX} / \theta_{JA}$$

θ_{JA} of the FT550 will be dependent on several variables: the packages used the thickness and size of the copper, the number of vias and the airflow. In the package, the FT550 uses the PSOP-8 with Power-PAD to improve the θ_{JA} . If the layout of the PCB can put a larger size of copper to contact the Power-PAD of this device, the θ_{JA} will be further improved. The better θ_{JA} is not only protecting the device well, but also increasing the maximum current capability at the same ambient temperature.

TYPICAL APPLICATION CIRCUITS

There are several application circuits shown in Figure 5 through 11 to illustrate some of the possible configurations of the FT550. Figure 5~7 are the SSTL-2 applications. For the majority of applications that implement the SSTL-2 termination scheme, it is recommended to connect all the input rails to 2.5V rail, as seen in Figure 6. This provides an optimal trade-off between power dissipation and component count.

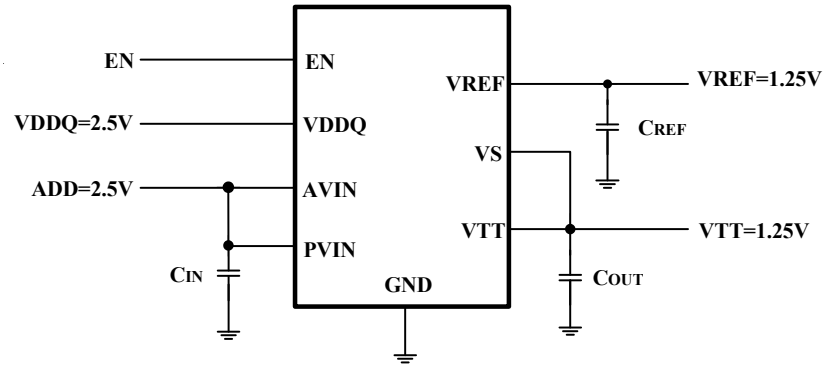


Figure 6: Recommended SSTL-2 Implementation

In Figure 7, the power rails are split. The power rail of the output stage (PVIN) can be as low as 1.8V; the power rail of the analog circuit (AVIN) is operated above 2V. The lower output stage power rail can lower the internal power dissipation when sourcing from the device and improve the efficiency, but the disadvantage is the maximum continuous current sourcing from VTT is reduced. This configuration is applied when the power dissipation and efficiency are concerned.

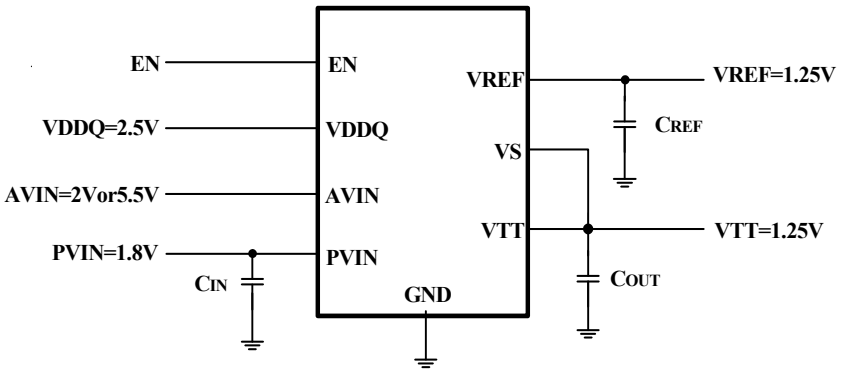


Figure 7: Lower Power Dissipation SSTL-2 Implementation

In Figure 8, the power rail of the output stage (PVIN) is connected to 3.3V to increase the maximum continuous current sourcing from VTT. AVIN should be always equal to or larger than PVIN. This configuration can increase the source capability of this device, but the power dissipation increases at the same time. It should be more careful to prevent the junction temperature from exceeding the maximum rating. Because of this risk, it is not recommended to supply the output stage power rail (PVIN) with a voltage higher than a nominal 3.3V rail.

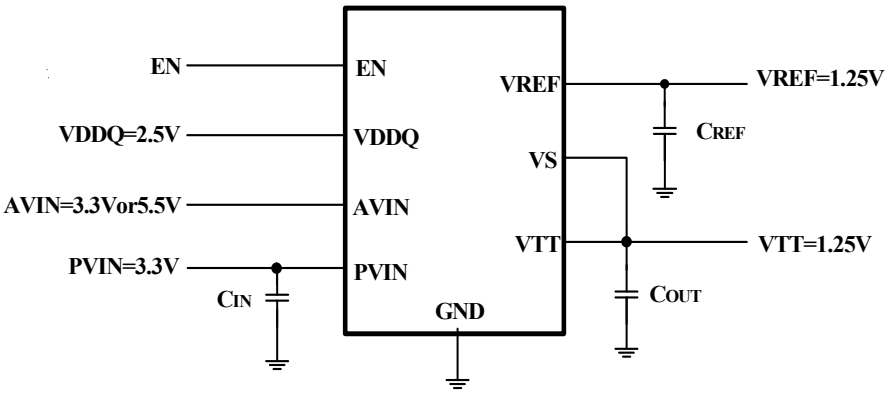


Figure 8: SSTL-2 Implementation with higher voltage rails

In Figure 9 & 10, they are the application configurations of DDR-II SDRAM bus terminations. Figure8 is the typical application scheme of DDR-II SDRAM. With the separate VDDQ pin and an internal resistor divider, it is possible to use the FT550 in applications utilizing DDR-II memory. Figure 9 is used to increase the driving capability. The risk is the same as figure 7.

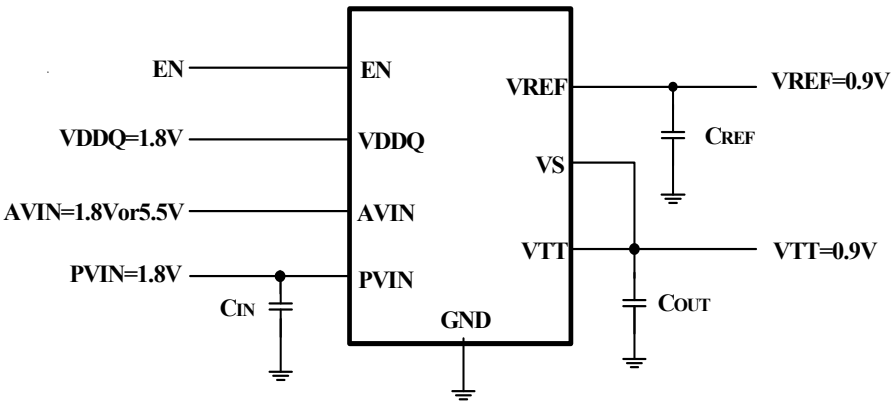


Figure 9: Recommended DDR-II Termination

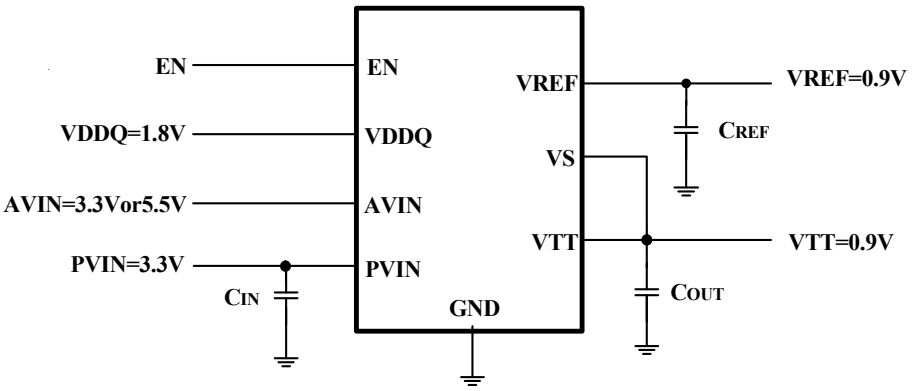


Figure 10: DR-II Termination with higher voltage rails

Figure 11 & 12 are used to scale the VTT to the wanted value when the standard voltages of SSTL-2 do not meet the requirements. Using R1 & R2, figure 10 can shift VTT up to VDDQ/2 * (1+R1/R2) and figure 11 can shift VTT down to VDDQ/2 * (1-R1/R2).

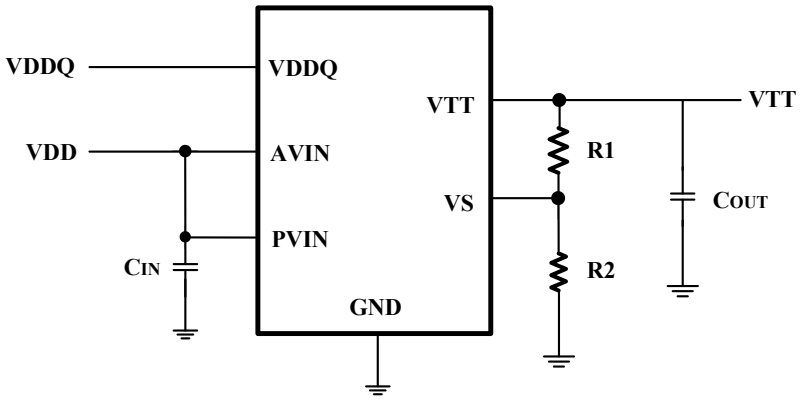


Figure 11: Increasing VTT by Level Shifting

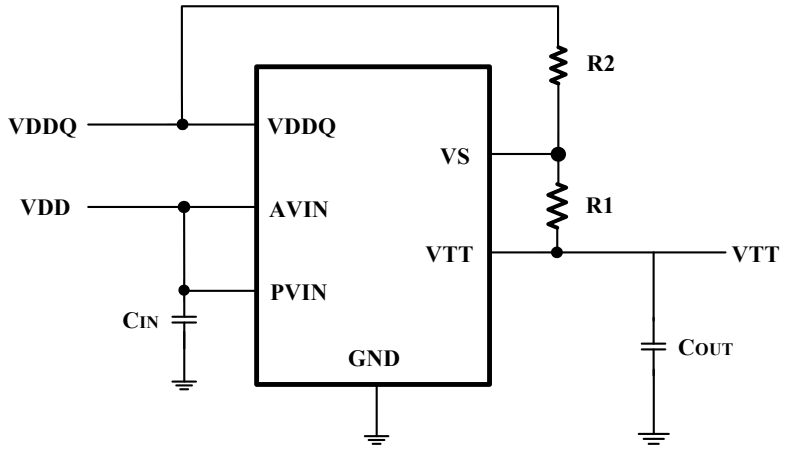
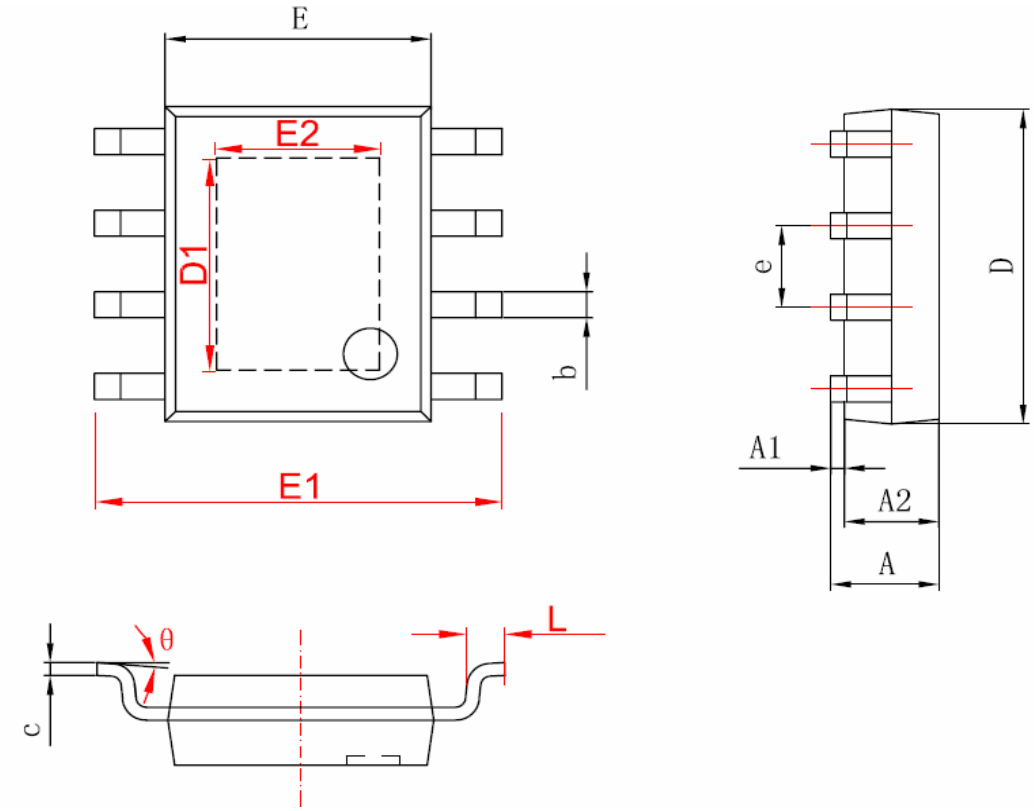


Figure 12: Decreasing VTT by Level Shifting

PAKAGING INFORMATION

PSOP-8(EXP PAD) PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Millimeters	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.05	0.15	0.004	0.01
A2	1.35	1.55	0.053	0.061
b	0.33	0.51	0.013	0.02
c	0.17	0.25	0.006	0.01
D	4.7	5.1	0.185	0.2
D1	3.202	3.402	0.126	0.134
E	3.8	4	0.15	0.157
E1	5.8	6.2	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.4	1.27	0.016	0.05
θ	0°	8°	0°	8°