

Dual Link DVI Receiver

EP263

User Guide

V0.5

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Explore Microelectronics, Taiwan

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Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Nov/21/2002	--	Initial Version
0.1	Nov/22/2002	--	Revised Version
0.2	Apr/11/2003	--	Pad Sequence Update
0.3	Sep/08/2003	--	Function Description Update: DCLK_POL: HIGH-rising to falling, LOW-falling to rising Power Dissipation
0.4	Dec/14/2004	Ether Lai	Update Power Dissipation & Add Package Dimension
0.5	Mar/24/2005	Ether Lai	Update LINK_ON specification

Section 1 Introduction

1.1 Overview

The EP263 is a low cost DVI receiver with Dual DVI links built in single 100-pin TQFP package. It is compliant to DVI Revision 1.0 specification and supports display resolution up to 330 M pixels/second. The build-in PLL requires no external component. The on-chip Link On detection circuit works even when the chip is put in Power Down mode. A Secondary Link Active detection circuit is also provide on-chip.

1.2 Features

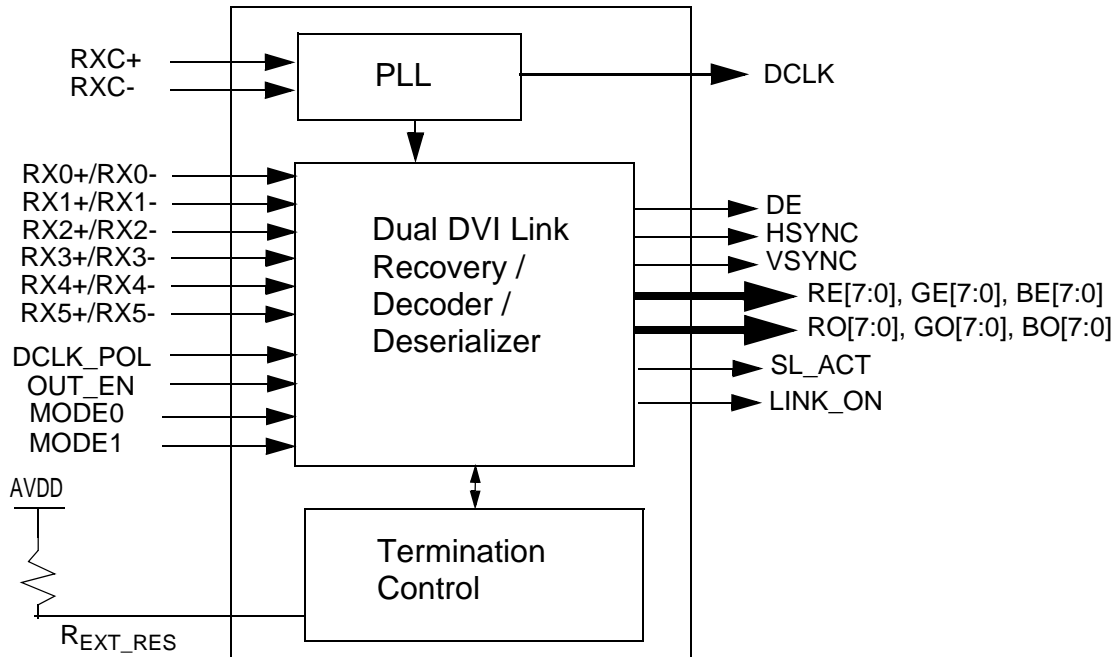
The DVI Receiver EP263 includes the following distinctive features:

- DVI specification 1.0 compliant
- Selection of Single-Link or Dual-Link operation
- Selection of Single-Port or Dual-Port output data in Single-Link mode
- Operation pixel rate: 25MHz - 330MHz
- PLL requires no external components
- High skew tolerance: 1 full input clock cycle for inter-channel within a link plus
1 full input clock cycle between links
- Low current consumption in Power Down mode
- Link On detection even in Power Down mode
- Secondary Link Active detection
- Controllable tri-state for output port
- Single 3.3V CMOS design
- 100-pin TQFP (Pb-Free, compliant to JEDEC/IPC J-STD-006)

Section 2 Overview

2.1 Block Diagram

Figure 2-1 Block Diagram of DVI Receiver EP263



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 Output Control/Data/CLK Pins

NAME	PIN #	IN/OUT	DESCRIPTION
R0E~R7E G0E~G7E B0E~B7E	43~49, 52 35~42 22~24, 27~31	OUT	Pixel Even Data Outputs. This data port corresponds to DVI receiver channel 0~2 in Dual-Link mode. When OUT_EN = LOW or MODE[1:0] = 00 the output drivers are placed in a high impedance state.
R0O~R7O G0O~G7O B0O~B7O	74, 77~83 66~73 56~63	OUT	Pixel Odd Data Outputs. This data port corresponds to DVI receiver channel 3~5 in Dual-Link mode. When OUT_EN = LOW or MODE[1:0] = 00 the output drivers are placed in a high impedance state.
DCLK	33	OUT	Data Clock Output. When OUT_EN = LOW or MODE[1:0] = 00 the output driver is placed in a high impedance state.
DE	53	OUT	Data Enable Output. When OUT_EN = LOW or MODE[1:0] = 00 the output driver is placed in a high impedance state.
HSYNC	55	OUT	Horizontal Sync Output. When OUT_EN = LOW or MODE[1:0] = 00 the output driver is placed in a high impedance state.
VSYNC	54	OUT	Vertical Sync Output. When OUT_EN = LOW or MODE[1:0] = 00 the output driver is placed in a high impedance state.
SL_ACT	21	OUT	Secondary Link Active Detect. The signal is only valid when the primary link is active. <ul style="list-style-type: none"> • HIGH Secondary Link is active. • LOW Secondary Link is not active.
LINK_ON	20	OUT	Link On Detect <ul style="list-style-type: none"> • HIGH DVI signals present and the link is active. • LOW DVI signals do not present and the link is off.

Table 2-2 Input Pins

NAME	PIN #	IN/OUT	DESCRIPTION
MODE[1:0]	17, 16	IN	<p>Operation Modes.</p> <ul style="list-style-type: none"> • 11 Dual Link with Dual Port data out. DVI receiver channel 0~2 data are output from R/G/B*E port. Channel 3~5 data are output from R/G/B*O port. • 10 Single Link with Dual Port data out. DVI receiver channel 3~5 are powered down. Even pixel data from channel 0~2 are output from R/G/B*E port. Odd pixel data are output from R/G/B*O port. • 01 Single Link with Single Port data out. DVI receiver channel 3~5 are powered down. Channel 0~2 data are output from R/G/B*E port. R/G/B*O port is not used. • 00 Power Down Mode. All the circuit is powered down except for the Link On detection circuit. DCLK, VSYNC, HSYNC, DE and all RGB outputs are put in tri-state.
OUT_EN	18	IN	<p>Output Enable. Pulled up by an internal resistor when left unconnected.</p> <ul style="list-style-type: none"> • HIGH Normal Operation. • LOW Put DCLK, VSYNC, HSYNC, DE and all RGB outputs in tri-state.
DCLK_POL	19	IN	<p>Data Clock Polarity.</p> <ul style="list-style-type: none"> • HIGH Outputs are triggered by falling edge of DCLK. • LOW Outputs are triggered by rising edge of DCLK.

Table 2-3 Reserved Pin

NAME	PIN #	IN/OUT	DESCRIPTION
RESERVED	84	IN	Must be tied HIGH for normal operation.

Table 2-4 Differential Signal Data Pins

NAME	PIN #	IN/OUT	DESCRIPTION
RX0+	87	Analog	Differential Data Input Pairs for Primary Link. (DVI v1.0 compliant)
RX0-	86		
RX1+	96		
RX1-	95		
RX2+	91		
RX2-	90		

Table 2-4 Differential Signal Data Pins

NAME	PIN #	IN/OUT	DESCRIPTION
RX3+ RX3- RX4+ RX4- RX5+ RX5-	10 9 5 4 14 13	Analog	Differential Data Input Pairs for Secondary Link. (DVI v1.0 compliant)
RXC+ RXC-	99 98	Analog	Differential Clock Input Pairs. (DVI v1.0 compliant)
EXT_RES	1	Analog	Impedance Matching Control. Resistor value is set ten times the termination resistance of each channel.

Table 2-5 Power and Ground Pins

NAME	PIN #	IN/OUT	DESCRIPTION
VDDI	34, 65	PWR	Internal VDD, 3.3V
VSSI	32, 64	GND	Internal Ground.
VDDE	26, 51, 76	PWR	Pad VDD, 3.3V
VSSE	25, 50, 75	GND	Pad Ground.
AVDD	88, 89, 93, 100, 7, 11, 12	PWR	Analog VDD, 3.3V
AVSS	85, 92, 94, 97, 6, 8, 15	GND	Analog Ground.
PVDD	2	PWR	PLL Analog VDD, 3.3V
PVSS	3	GND	PLL Analog Ground.

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}^1	Supply Voltage	-0.3		4.0	V
V_I	Input Voltage	-0.3		$V_{CC} + 0.3$	V
V_O^2	Output Voltage	-0.3		$V_{CC} + 0.3$	V
T_A	Ambient Temperature (with power applied)	-25		125	°C
T_{STG}	Storage Temperature	-65		150	°C
	Thermal Resistance (Junction to Ambient)		21		°C/W

NOTES:

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV _{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage ¹	$I_{CL} = -18mA$			GND - 0.8	V
V_{CIPL}	Input Clamp Voltage ¹	$I_{CL} = 18mA$			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage ¹	$I_{CL} = -18mA$			GND - 0.8	V
V_{COPL}	Output Clamp Voltage ¹	$I_{CL} = 18mA$			OVCC + 0.8	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

NOTES:

1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3ns or one third of the clock cycle.

DC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{OHD}	Output High Drive Data and Controls	V _{OUT} = 1.2V	7.0	12.0		mA
I _{OLD}	Output Low Drive Data and Controls	V _{OUT} = 0.8V	-7.0	-12.0		mA
V _{ID}	Differential Input Voltage, Single Ended Amplitude		75		1000	mV
I _{PD}	Power-Down Current	PWR_UP = LOW No RXC+/- input		7		mA
I _{CCR}	Receiver Supply Current	DCLK=165MHz, MODE[1:0] = 2'b11 C _{LOAD} = 10pF R _{EXT_SWING} = 510 ohm Typical Pattern ¹		331		mA
		Worst Case Pattern ²		536		mA

NOTES:

1. The typical Pattern contains a gray scale area, checkerboard area and text
2. Black and white checkerboard pattern, each checker is two pixels wide.

AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T _{DPS}	Intra-Pair (+ to -) Differential Input Skew ¹	165 MHz			245	ps
T _{CCS}	Channel to Channel Differential Input Skew ¹	165 MHz			4	ns
T _{IJIT}	Worst Case Differential Input Clock Jitter Tolerance ^{2,3}	65 MHz			465	ps
		112 MHz			270	ps
		165 MHz			182	ps
D _{LHT}	Low-to-High Transition Time: DCLK, Data and Controls (70°C, 165MHz)	C _L = 10pF			2.4	ns
D _{HLT}	High-to-Low Transition Time: DCLK, Data and Controls (70°C, 165MHz)	C _L = 10pF			2.3	ns
T _{SETUP}	Data, DE, VSYNC, HSYNC and CTL[3:0] Setup Time to DCLK active edge at 165MHz	C _L = 10pF	1.0			ns
T _{HOLD}	Data, DE, VSYNC, HSYNC and CTL[3:0] Hold Time from DCLK active edge	C _L = 10pF	1.5			ns
T _{CIP}	DCLK Cycle Time		6.06		40	ns

F _{CIP}	DCLK Frequency		25		165	MHz
T _{CIH}	DCLK High Time ⁴	C _L = 10pF	1.7			ns
T _{CIL}	DCLK Low Time ⁴	C _L = 10pF	2.0			ns
T _{PDL}	Delay from OUT_EN Low to High Impedance outputs				10	ns
T _{LINK_OFF}	Link Disabled (Tx power down) to LINK_ON Low ⁵				10	ms
T _{LINK_ON}	Link Enabled (Clock Present) to LINK_ON High				10	ms

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronical Measurement Procedures*
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5. Measured when transmitter was powered down and no TMDS clock presented.

2.5 Timing Diagrams

Figure 2-3 Digital Output Transition Timing Definition

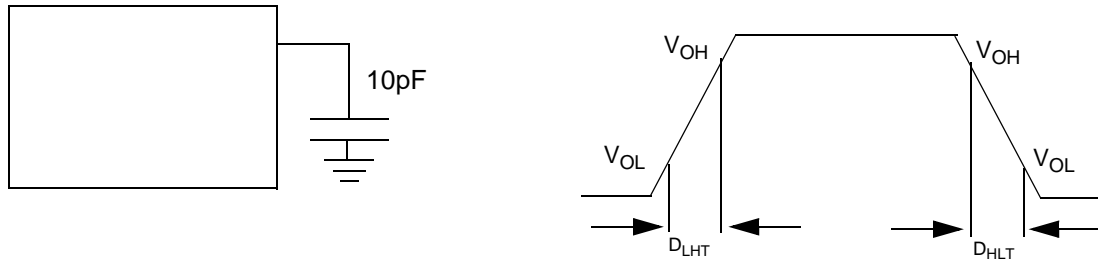


Figure 2-4 Clock Cycle and High/Low Timing Definition

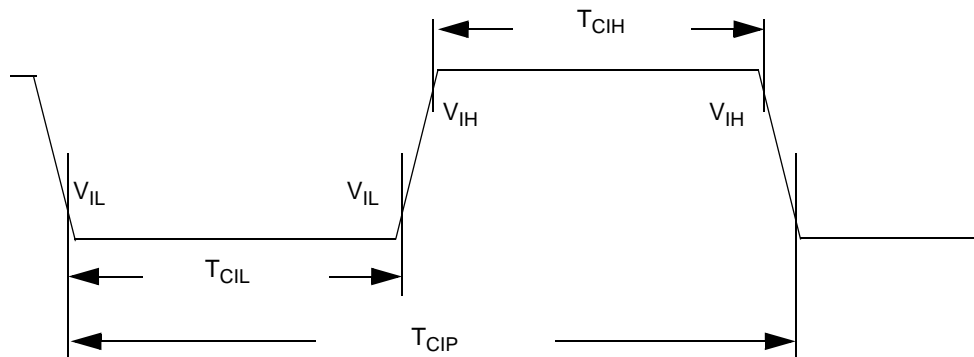


Figure 2-5 Channel to Channel Skew Timing Definition

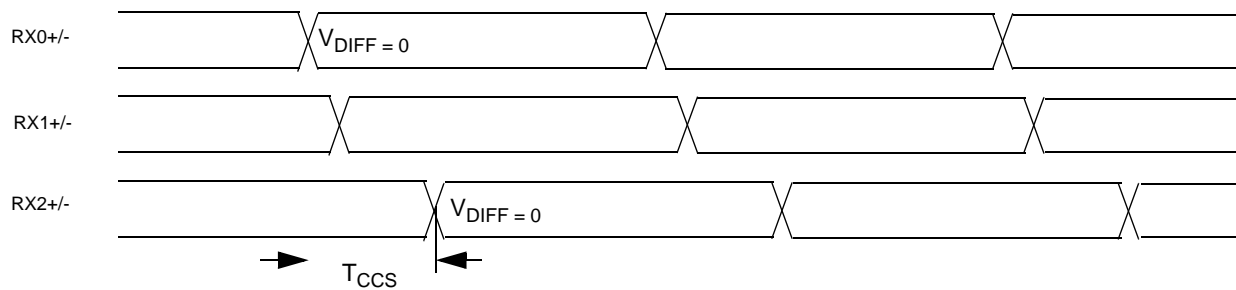


Figure 2-6 Output to DCLK Timing Definition

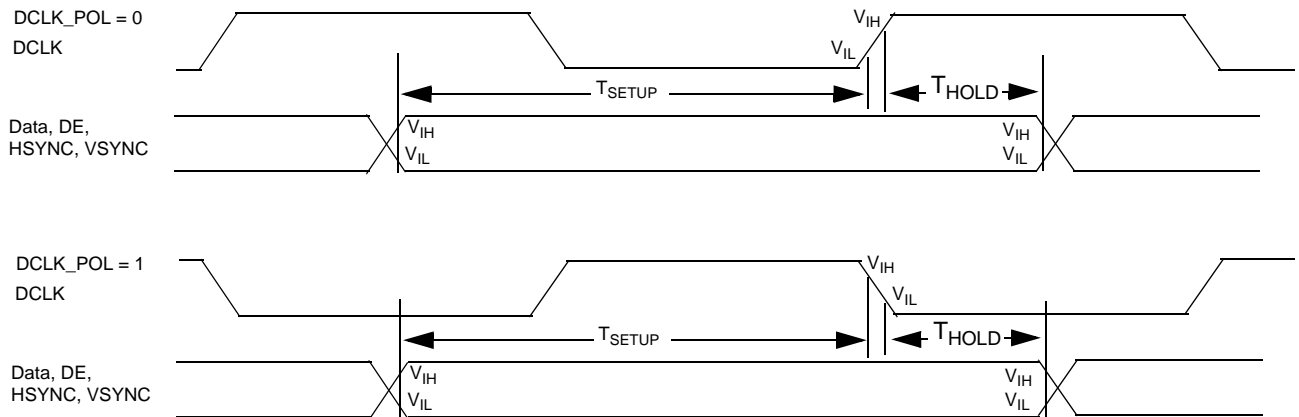


Figure 2-7 LINK_ON Output Timing Definition

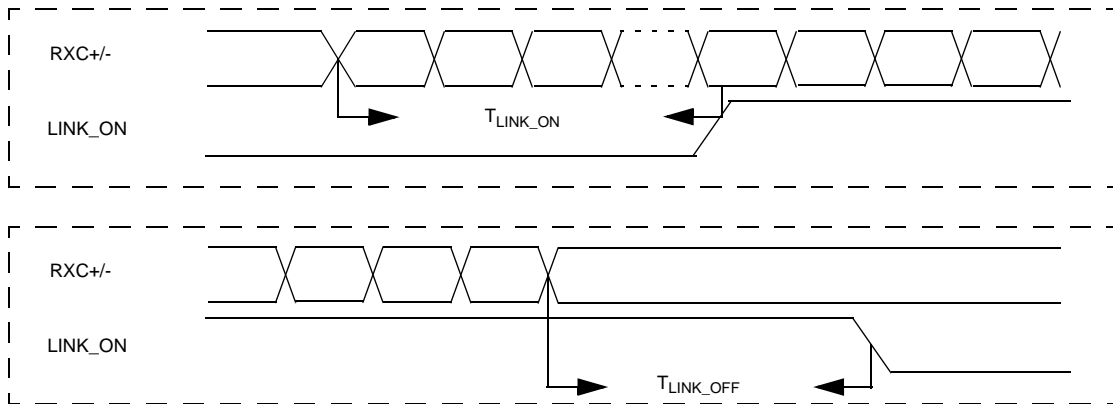
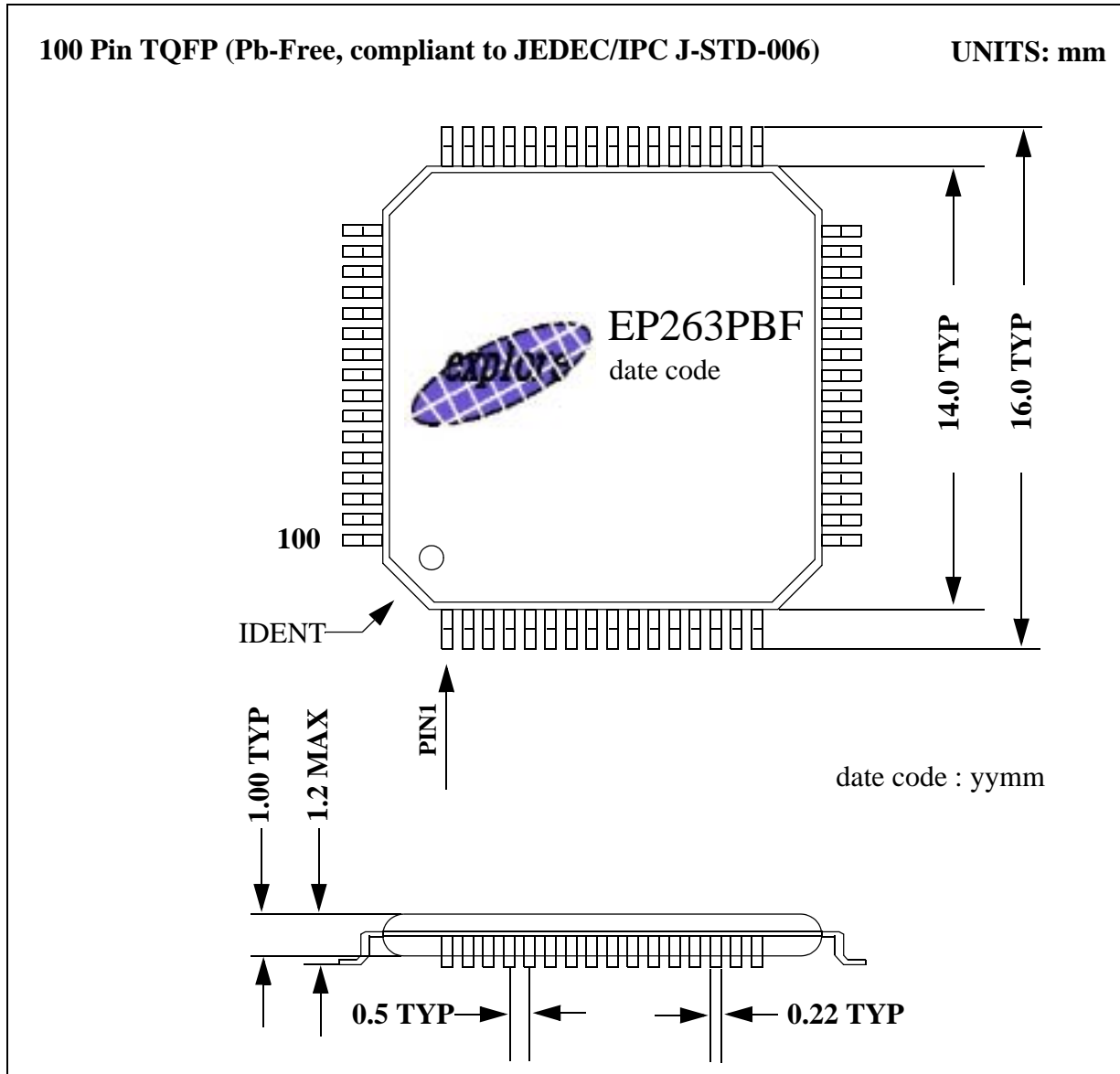


Figure 2-8 OUT_EN to Output Signals Disabled Timing Definition



Section 3 Package

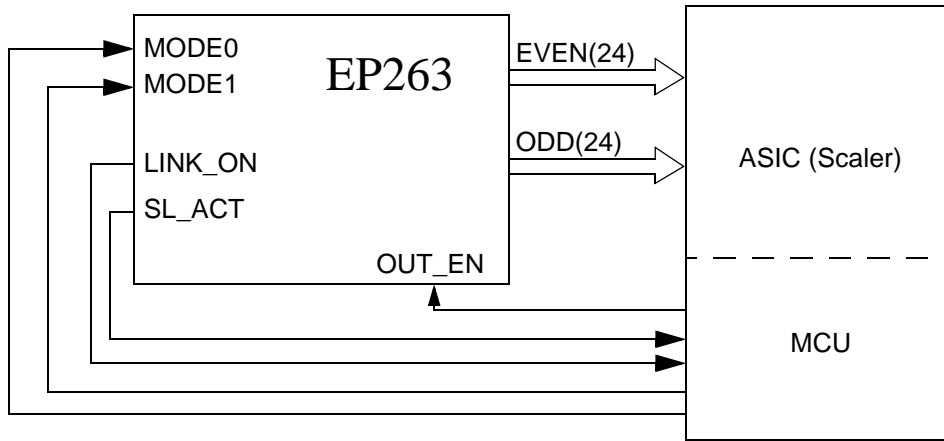


Appendix A Suggested Mode Change Algorithm

The EP263 can support up to 330MHz (dual DVI links input) bandwidth. The operation mode has to setup carefully for the correct display. The suggested circuit and algorithm to handle the mode control register (MODE[1:0]) is shown below:

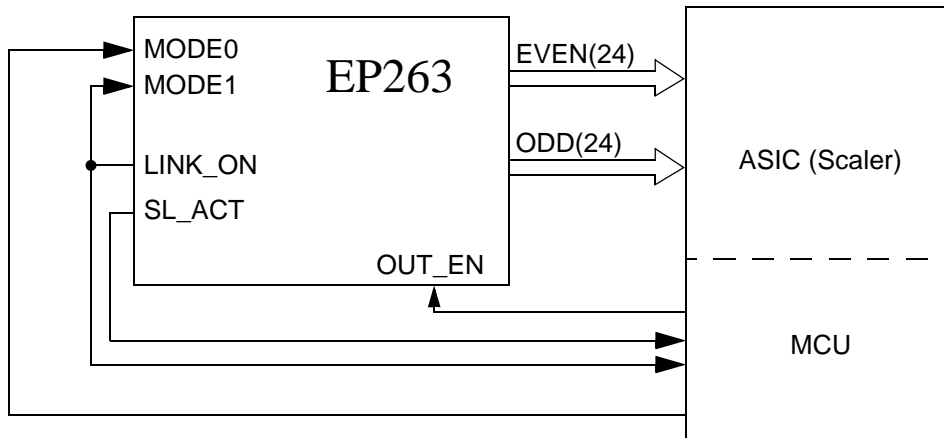
The following circuit block diagram shows the configuration of the EP263 status and control pins. In this example, the EP263 can be configured as Dual Link with Dual Port data out (MODE[1:0] = 2'b11), Single Link with Dual Port data out (MODE[1:0] = 2'b10) or Single Link with Single Port data out (MODE[1:0] = 2'b01).

Figure A-1 Circuit Block Diagram



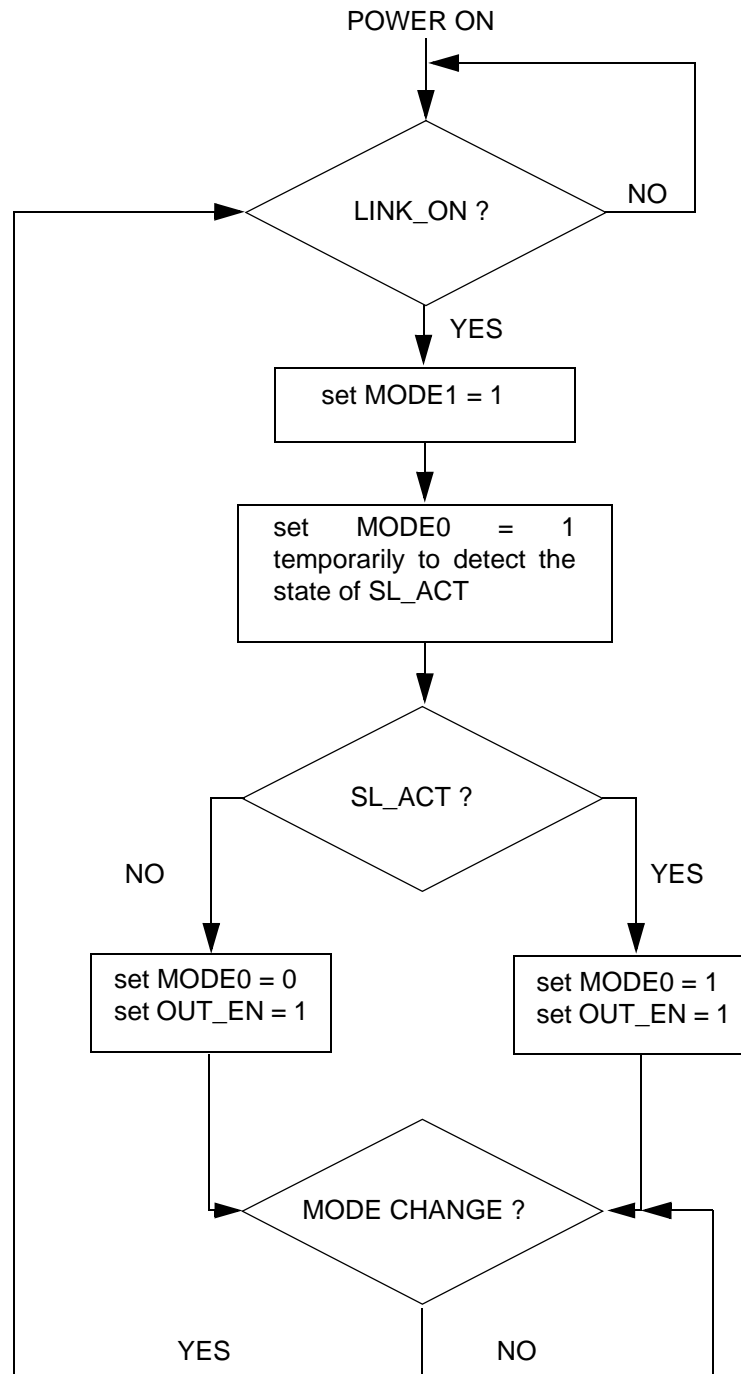
The following alternate circuit block diagram shows the configuration of the EP263 status and control pins. In this example, the EP263 can be configured as Dual Link with Dual Port data out (MODE[1:0] = 2'b11) and Single Link with Dual Port data out (MODE[1:0] = 2'b10) only. The advantage of this alternate circuit is to save the needed MCU I/O pin.

Figure A-2 Alternate Circuit Block Diagram



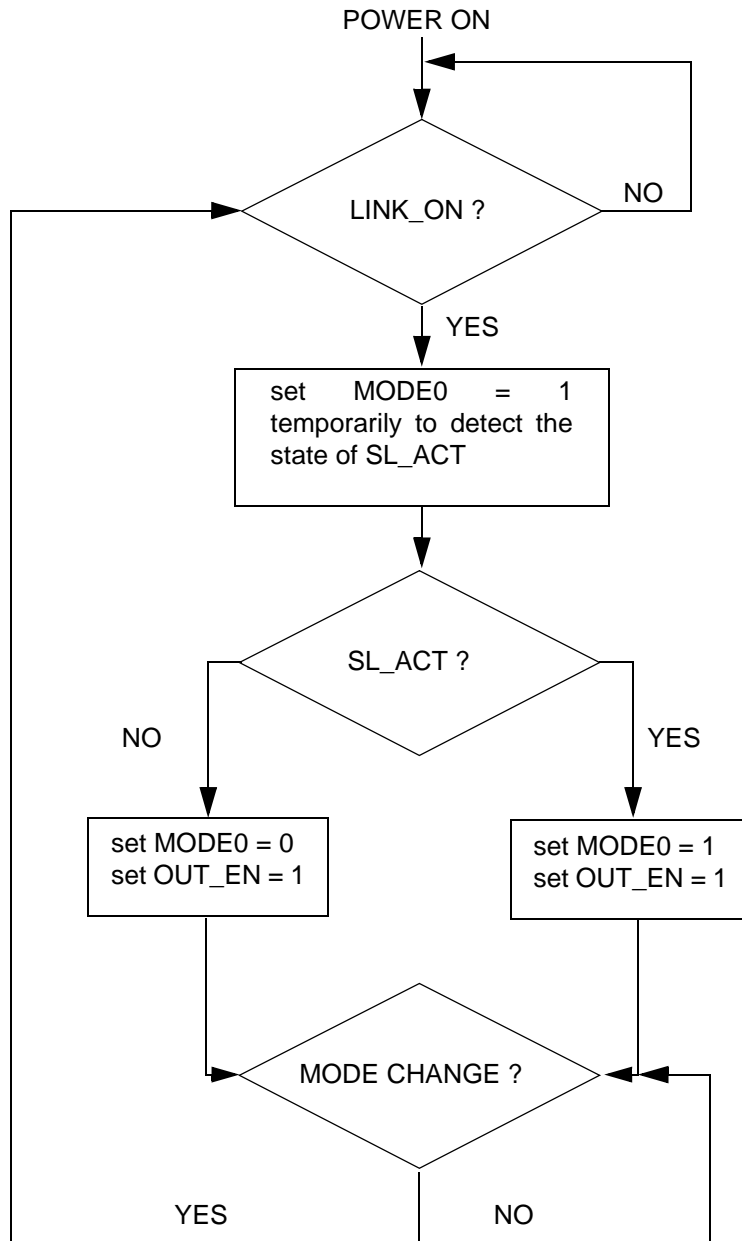
The following flowchart shows the MCU flow to control the mode change of circuit Figure A-1:

Figure A-3 MCU FlowChart



The following flowchart shows the alternate MCU flow to control the mode change of circuit Figure A-2:

Figure A-4 Alternate MCU FlowChart



User Guide End Sheet

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