

DVI Compliant Receiver EP261

User Guide V0.2

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Explore Microelectronics, Taiwan

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Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Jun/06/2002	--	Initial Version
0.1	Aug/19/2002	--	Revised Version
0.2	Apr/01/2003	--	Revised Version

Section 1 Introduction

1.1 Overview

The EP261 is a low cost DVI receiver in 64-pin LQFP package. It is compliant to DVI Rev 1.0 specification and supports display resolution from VGA to SXGA (25 - 135MHz), up to 24 bit/pixel. The build-in PLL requires no external component. The on-chip Link On detection circuit works even when the chip is put in Power Down mode.

1.2 Features

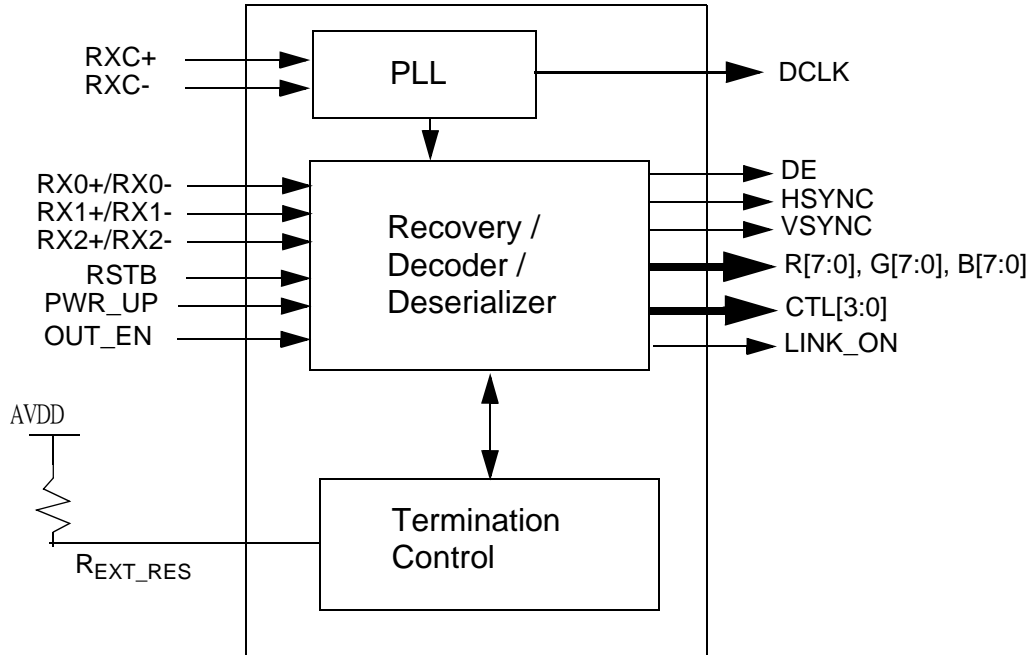
The DVI Receiver EP261 includes these distinctive features:

- DVI specification 1.0 compliant
- Operation pixel frequency range: 25MHz - 135MHz
- PLL requires no external components
- High skew tolerance: 1 full input clock cycle
- Low current consumption in Power Down mode
- Link On detection even in Power Down mode
- Controllable tri-state for output port
- Single 3.3V CMOS design
- 64-pin LQFP

Section 2 Overview

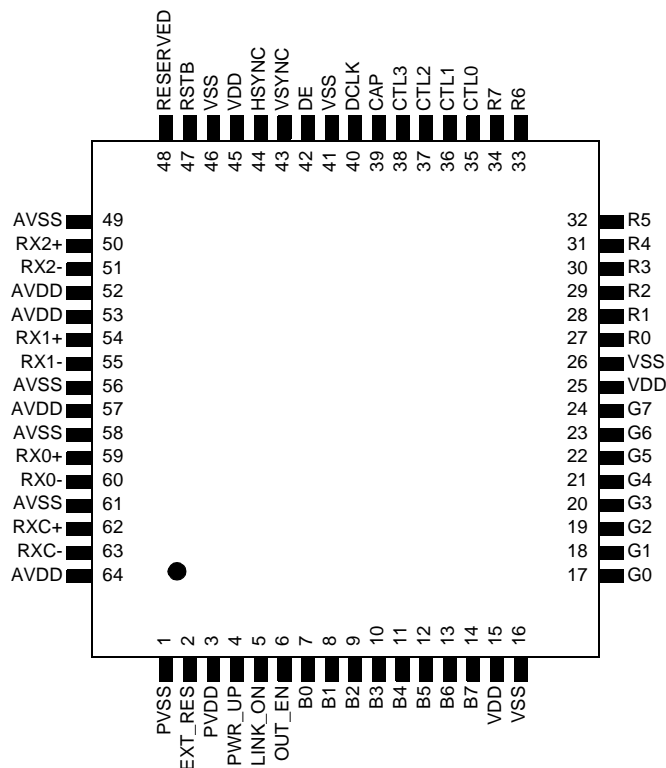
2.1 Block Diagram

Figure 2-1 Block Diagram of DVI Receiver EP261



2.2 Pin Diagram

Figure 2-2 Pin Diagram of DVI Receiver



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 Output Control/Data/CLK Pins

NAME	PIN #	IN/OUT	DESCRIPTION
R0~R7 G0~G7 B0~B7	27~34 17~24 7~14	OUT	Pixel Data Outputs. When OUT_EN = LOW the output drivers are placed in a high impedance state.
DCLK	40	OUT	Pixel Clock Output. When OUT_EN = LOW the output driver is placed in a high impedance state.
DE	42	OUT	Data Enable Output. When OUT_EN = LOW the output driver is placed in a high impedance state.

Table 2-1 Output Control/Data/CLK Pins

NAME	PIN #	IN/OUT	DESCRIPTION
HSYNC	44	OUT	Horizontal Sync Output. When OUT_EN = LOW the output driver is placed in a high impedance state.
VSYNC	43	OUT	Vertical Sync Output. When OUT_EN = LOW the output driver is placed in a high impedance state.
CTL0 - CTL3	35~38	OUT	Decoded DVI Control Signal Outputs
LINK_ON	5	OUT	Link On Detect <ul style="list-style-type: none"> • HIGH DVI signals present and the link is active. • LOW DVI signals do not present and the link is off.

Table 2-2 Input Pins

NAME	PIN #	IN/OUT	DESCRIPTION
RSTB	47	IN	External Reset. <ul style="list-style-type: none"> • HIGH or Open Normal Operation. • LOW Chip reset.
PWR_UP	4	IN	Power Up. <ul style="list-style-type: none"> • HIGH Normal Operation. • LOW Power Down Mode. All the circuit is powered down except for the Link On detection circuit.
OUT_EN	6	IN	Output Enable. <ul style="list-style-type: none"> • HIGH Normal Operation. • LOW Put DCLK, VSYNC, HSYNC, DE and all RGB outputs in tri-state.

Table 2-3 Reserved Pin

NAME	PIN #	IN/OUT	DESCRIPTION
RESERVED	48	IN	Must be tied LOW for normal operation.

Table 2-4 Differential Signal Data Pins

NAME	PIN #	IN/OUT	DESCRIPTION
RX0+	59	Analog	Differential Data Input Pairs. (DVI v1.0 compliant)
RX0-	60		
RX1+	54		
RX1-	55		
RX2+	50		
RX2-	51		

Table 2-4 Differential Signal Data Pins

NAME	PIN #	IN/OUT	DESCRIPTION
RXC+ RXC-	62 63	Analog	Differential Clock Input Pairs. (DVI v1.0 compliant)
EXT_RES	2	Analog	Impedance Matching Control. Resistor value is set ten times the termination resistance of each channel.

Table 2-5 Power and Ground Pins

NAME	PIN #	IN/OUT	DESCRIPTION
VDD	15, 25, 45	PWR	Digital VDD, 3.3V
VSS	16, 26, 46, 41	GND	Digital Ground.
AVDD	52, 53, 57, 64	PWR	Analog VDD, 3.3V
AVSS	49, 56, 58, 61	GND	Analog Ground.
PVDD	3	PWR	PLL Analog VDD, 3.3V
PVSS	1	GND	PLL Analog Ground.
CAP	39		A 10 uF capacitor for internal regulator is required to connect between this pin and Digital Ground.

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{CC} ¹	Supply Voltage	-0.3		4.0	V
V _I	Input Voltage	-0.3		V _{CC} + 0.3	V
V _O ²	Output Voltage	-0.3		V _{CC} + 0.3	V
T _A	Ambient Temperature (with power applied)	-25		125	°C
T _{STG}	Storage Temperature	-65		150	°C
	Thermal Resistance (Junction to Ambient)		21		°C/W

NOTES:

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{CC}	Supply Voltage	3.0	3.3	3.6	V
V _{CCN}	Supply Voltage Noise			100	mV _{p-p}
T _A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IH}	High-level Input Voltage		2.0			V
V _{IL}	Low-level Input Voltage				0.8	V
V _{OH}	High-level Output Voltage		2.4			V
V _{OL}	Low-level Output Voltage				0.4	V
V _{CINL}	Input Clamp Voltage ¹	I _{CL} = -18mA			GND - 0.8	V
V _{CIPL}	Input Clamp Voltage ¹	I _{CL} = 18mA			IVCC + 0.8	V
V _{CONL}	Output Clamp Voltage ¹	I _{CL} = -18mA			GND - 0.8	V
V _{COPL}	Output Clamp Voltage ¹	I _{CL} = 18mA			OVCC + 0.8	V
I _{OL}	Output Leakage Current	High Impedance	-10		10	uA

NOTES:

1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3ns or one third of the clock cycle.

DC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _{OHD}	Output High Drive Data and Controls	V _{OUT} = 1.2V	7.0	12.0		mA
I _{OLD}	Output Low Drive Data and Controls	V _{OUT} = 0.8V	-7.0	-12.0		mA
V _{ID}	Differential Input Voltage, Single Ended Amplitude		75		1000	mV
I _{PD}	Power-Down Current	PWR_UP = LOW No RXC+/- input		6		mA
I _{CLKI}	Power-Down Current	PWR_UP = HIGH No RXC+/- input		58		mA
I _{PDO}	Receiver Supply Current with Outputs Disabled	DCLK=135MHz, C _{LOAD} = 10pF R _{EXT_SWING} = 390 ohm OUT_EN = LOW		165		mA
I _{CCR}	Receiver Supply Current	DCLK=135MHz, C _{LOAD} = 10pF R _{EXT_SWING} = 390 ohm Typical Pattern ¹		180		mA
		Worst Case Pattern ²		215		mA

NOTES:

1. The typical Pattern contains a gray scale area, checkerboard area and text
2. Black and white checkerboard pattern, each checker is two pixels wide.

AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T _{DPS}	Intra-Pair (+ to -) Differential Input Skew ¹	135 MHz			245	ps
T _{CCS}	Channel to Channel Differential Input Skew ¹	135 MHz			4	ns
T _{IJIT}	Worst Case Differential Input Clock Jitter Tolerance ^{2,3}	65 MHz			465	ps
		112 MHz			270	ps
		135 MHz			182	ps
D _{LHT}	Low-to-High Transition Time: DCLK, Data and Controls (70°C, 135MHz)	C _L = 10pF			2.4	ns
D _{HLT}	High-to-Low Transition Time: DCLK, Data and Controls (70°C, 135MHz)	C _L = 10pF			2.3	ns

T _{SETUP}	Data, DE, VSYNC, HSYNC and CTL[3:0] Setup Time to DCLK rising edge at 135MHz	C _L = 10pF	3.0			ns
T _{HOLD}	Data, DE, VSYNC, HSYNC and CTL[3:0] Hold Time from DCLK rising edge	C _L = 10pF	1.0			ns
T _{CIP}	DCLK Cycle Time		7.4		40	ns
F _{CIP}	DCLK Frequency		25		135	MHz
T _{CIH}	DCLK High Time ⁴	C _L = 10pF	1.7			ns
T _{CIL}	DCLK Low Time ⁴	C _L = 10pF	2.0			ns
T _{PDL}	Delay from OUT_EN Low to High Impedance outputs				10	ns
T _{HSC}	Link Disabled (Tx power down) to LINK_ON Low ⁵				250	ms
T _{FSC}	Link Enabled (DE Active) to LINK_ON High ¹			25	40	DE edges

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronical Measurement Procedures*
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5. Measured when transmitter was powered down.

Setup Time for data rates other than 135MHz:

The measurements shown above is the minimum setup time based on the maximum data rate of 135MHz. To estimate the setup times for the other slower data rates, the following formula can be used:

$$\text{Time (new frequency)} = \text{Time (135MHz)} + (\text{Clock Period at new frequency} - \text{Clock Period at 135MHz})$$

2.5 Timing Diagrams

Figure 2-3 Digital Output Transition Timing Definition

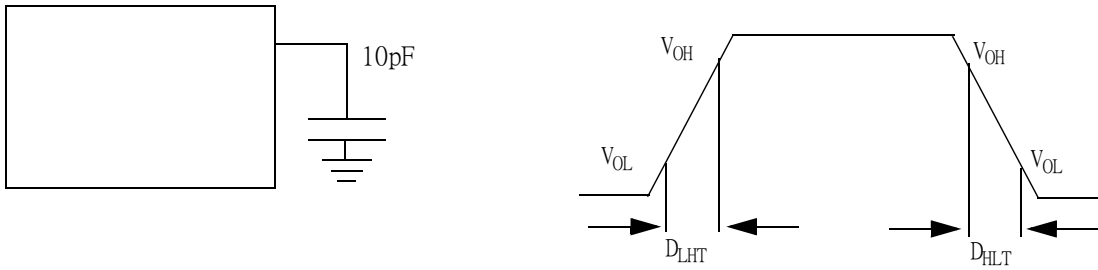


Figure 2-4 Clock Cycle and High/Low Timing Definition

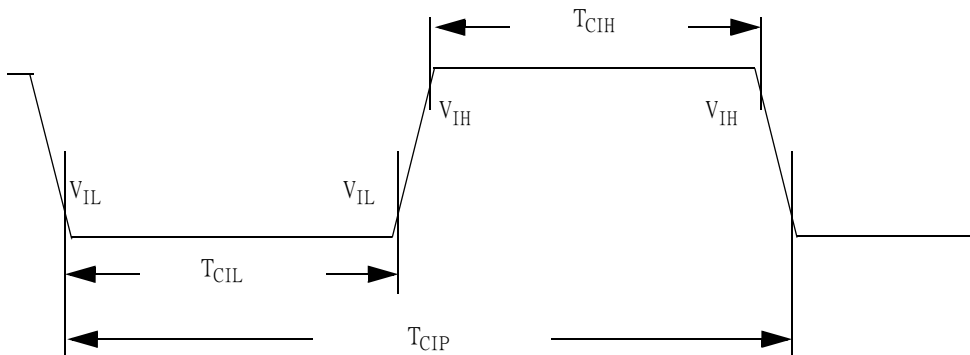


Figure 2-5 Channel to Channel Skew Timing Definition

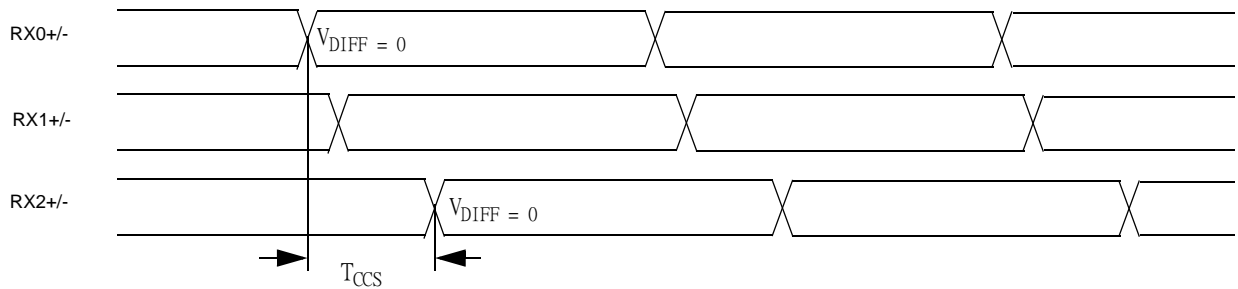


Figure 2-6 Output to DCLK Timing Definition

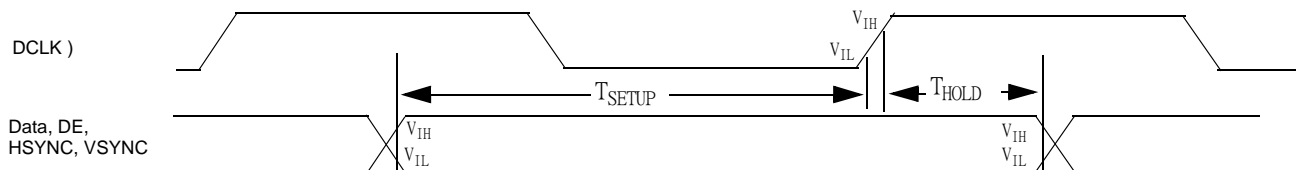
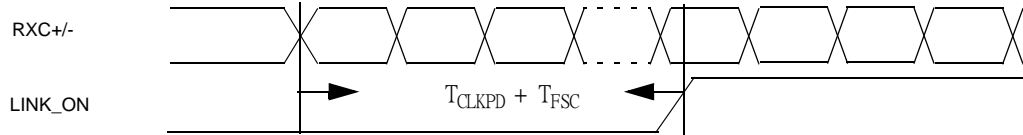


Figure 2-7 Wake Up on Clock Detected Timing Definition**Figure 2-8 OUT_EN to Output Signals Disabled Timing Definition**

User Guide End Sheet

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