DVI + HDCP Compliant Receiver
EP169

User Guide
V0.6

Revised: Mar. 04, 2005

Original Release Date: July 08, 2003

Explore Microelectronics, Taiwan

Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Jul/08/2003	--	Initial Version
0.1	Jul/22/2003	--	Revised Version -- EEPROM Application
0.2	Jan/12/2004	Ether Lai	Remove the HDCP+EDID combination function Redefine the "EDID_EXC" to "RESERVED" Pin
0.3	Mar/16/2004	Ether Lai	Fill the power consumption
0.4	Aug/04/2004	Ether Lai	Fix Typos
0.5	Dec/14/2004	Ether Lai	Update Electrical Characteristics & Add Package Information
0.6	Mar/04/2005	Ether Lai	Update LINK_ON specification

Section 1 Introduction

1.1 Overview

The EP169 is a low cost DVI receiver integrated with HDCP (High-bandwidth Digital Content Protection) engine in 100-pin LQFP package. It is compliant to DVI Revision 1.0 and HDCP Revision 1.0 specifications. HDCP keys are encrypted and put in an external EEPROM. The chip supports display resolution from VGA to UXGA (25 - 165MHz) in 1 or 2 pixels/clock mode. The on-chip Link On detection circuit works even when the chip is put in Power Down mode.

1.2 Features

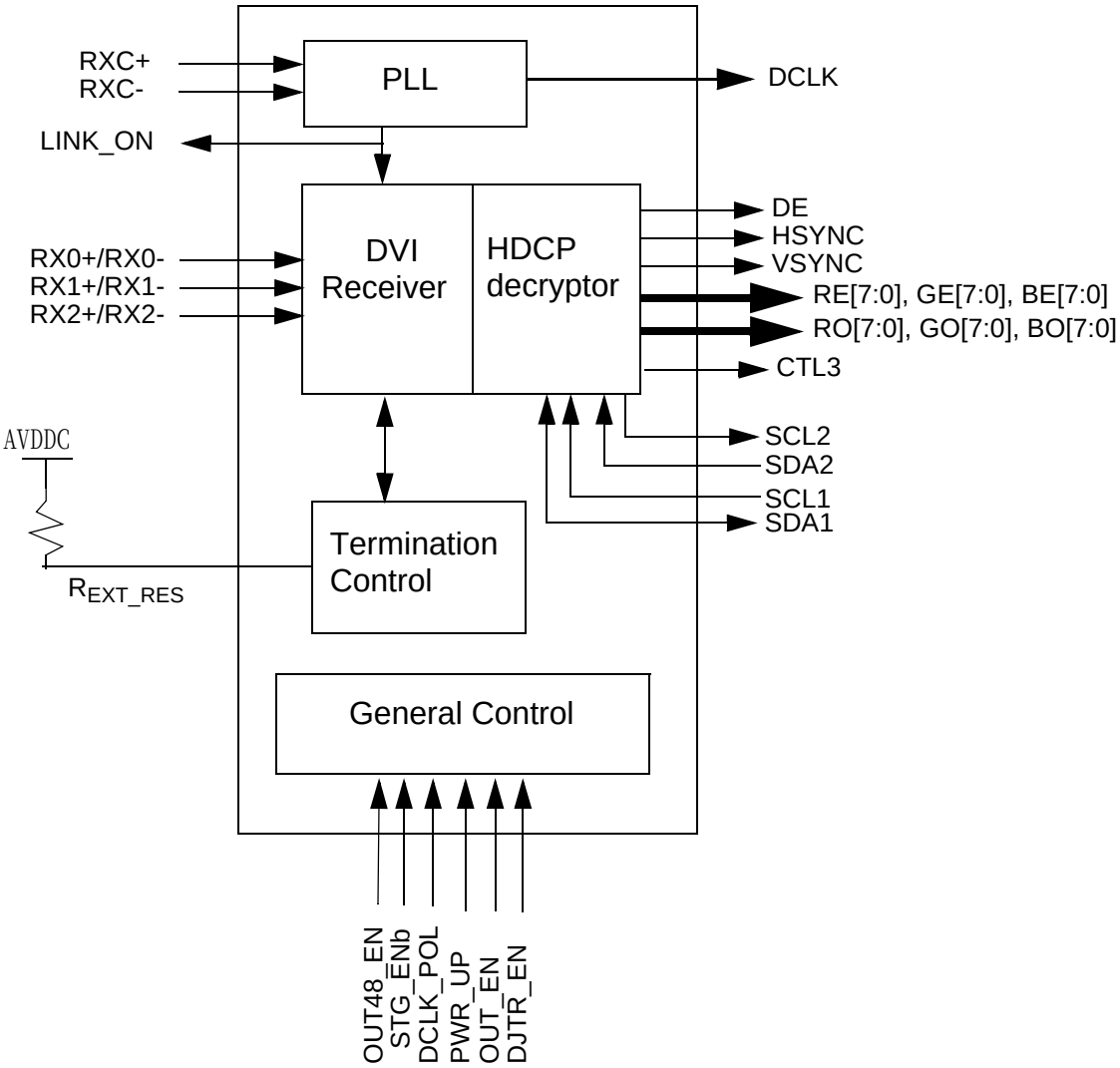
The DVI Receiver EP169 includes these distinctive features:

- DVI specification 1.0 compliant
- HDCP specification 1.0 compliant
- Operation pixel frequency range: 25MHz - 165MHz
- Encrypted HDCP keys store in external EEPROM
- PLL requires no external components
- High skew tolerance: 1 full input clock cycle
- H/V sync de-jittering
- Low current consumption in Power Down mode
- Link On detection even in Power Down mode
- Controllable tri-state for output port
- Backward compatible with EP161
- Single 3.3V CMOS design
- 100-pin LQFP Package (Pb-free, compliant to JEDEC/IPC J-STD-006)

Section 2 Overview

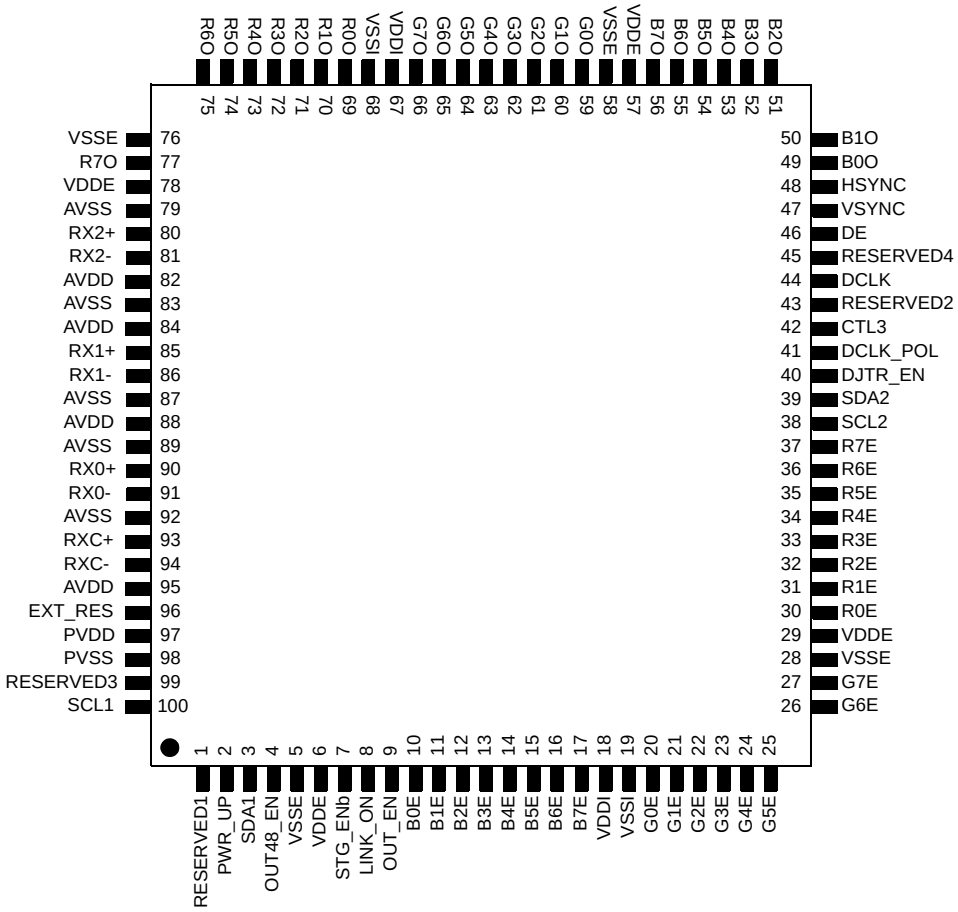
2.1 Block Diagram

Figure 2-1 Block Diagram of EP169



2.2 Pin Diagram

Figure 2-2 Pin Diagram of DVI Receiver



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 Output Control/Data/CLK Pins

NAME	PIN #	IN/OUT	DESCRIPTION
R0E~R7E G0E~G7E B0E~B7E	30~37 20~27 10~17	OUT	Pixel Even Data Outputs. When OUT_EN = LOW or PWR_UP = LOW the output drivers are placed in a high impedance state.

Table 2-1 Output Control/Data/CLK Pins

NAME	PIN #	IN/OUT	DESCRIPTION
R0O~R7O G0O~G7O B0O~B7O	69~75, 77 59~66 49~56	OUT	Pixel Odd Data Outputs. When OUT_EN = LOW or PWR_UP = LOW the output drivers are placed in a high impedance state.
DCLK	44	OUT	Data Clock Output. When OUT_EN = LOW or PWR_UP = LOW the output driver is placed in a high impedance state.
DE	46	OUT	Data Enable Output. When OUT_EN = LOW or PWR_UP = LOW the output driver is placed in a high impedance state.
HSYNC	48	OUT	Horizontal Sync Output. When OUT_EN = LOW or PWR_UP = LOW the output driver is placed in a high impedance state.
VSYNC	47	OUT	Vertical Sync Output. When OUT_EN = LOW or PWR_UP = LOW the output driver is placed in a high impedance state.
CTL3	42	OUT	Decoded DVI Control Signal 3 Output
LINK_ON	8	OUT	Link On Detect • **HIGH** DVI signals present and the link is active. • **LOW** DVI signals do not present and the link is off.

Table 2-2 Input Pins

NAME	PIN #	IN/OUT	DESCRIPTION
PWR_UP	2	IN	Power Up. • **HIGH** Normal Operation. • **LOW** Power Down Mode. All the circuit is powered down except for the Link On detection circuit. DCLK, VSYNC, HSYNC, DE, CTL3 and all RGB outputs are put in tri-state.
OUT_EN	9	IN	Output Enable. Pulled up by an internal resistor when left unconnected. • **HIGH** Normal Operation. • **LOW** Put DCLK, VSYNC, HSYNC, DE, CTL3 and all RGB outputs in tri-state.
OUT48_EN	4	IN	Dual Pixel Output Enable. • **HIGH** 2 pixels are output per DCLK using R/G/BxE for 1st pixel and R/G/BxO for 2nd pixel. • **LOW** 1 pixel is output per DCLK using R/G/BxE.

Table 2-2 Input Pins

NAME	PIN #	IN/OUT	DESCRIPTION
STG_ENb	7	IN	Staggered Output Enable. Active low. • **HIGH** Selects normal simultaneous outputs on all even and odd data lines. • **LOW** Selects staggered output drive by delaying even data lines by 1/4 DCLK cycle. This function is only available when OUT48_EN = HIGH.
DJTR_EN	40	IN	HSYNC/VSYNC De-Jittering Enable. • **HIGH** HSYNC/VSYNC Outputs are de-jittered and maintain fixed timing relationship with DE output. 1 to 3 pixel clock delay may be added to HSYNC/VSYNC outputs. • **LOW** HSYNC/VSYNC Outputs are not de-jittered.
DCLK_POL	41	IN	Data Clock Polarity. • **HIGH** Outputs are triggered by rising edge of DCLK. • **LOW** Outputs are triggered by falling edge of DCLK.

Table 2-3 IIC Pin

NAME	PIN #	IN/OUT	DESCRIPTION
SCL1	100	IN	IIC clock input from DDC.
SDA1	3	IN/OUT	IIC data input/output from/to DDC.
SCL2	38	OUT	IIC clock output to external EE. An external 10K ohm pull up is required.
SDA2	39	IN/OUT	IIC data input/output from/to external EE. An external 10K ohm pull up is required.

Table 2-4 Reserved Pin

NAME	PIN #	IN/OUT	DESCRIPTION
RESERVED1	1	IN	Must be tied HIGH for normal operation.
RESERVED2	43	IN	Must be tied HIGH for normal operation.
RESERVED3	99	IN	Must be tied HIGH for normal operation.
RESERVED4	45	IN	Must be tied LOW for normal operation.

Table 2-5 Differential Signal Data Pins

NAME	PIN #	IN/OUT	DESCRIPTION
RX0+ RX0- RX1+ RX1- RX2+ RX2-	90 91 85 86 80 81	Analog	Differential Data Input Pairs. (DVI v1.0 compliant)

Table 2-5 Differential Signal Data Pins

NAME	PIN #	IN/OUT	DESCRIPTION
RXC+ RXC-	93 94	Analog	Differential Clock Input Pairs. (DVI v1.0 compliant)
EXT_RES	96	Analog	Impedance Matching Control. Resistor value is set ten times the termination resistance of each channel.

Table 2-6 Power and Ground Pins

NAME	PIN #	IN/OUT	DESCRIPTION
VDDI	18, 67	PWR	Internal VDD, 3.3V
VSSI	19, 68	GND	Internal Ground.
VDDE	6, 29, 57, 78	PWR	Pad VDD, 3.3V
VSSE	5, 28, 58, 76	GND	Pad Ground.
AVDD	82, 84, 88 95	PWR	Analog VDD, 3.3V
AVSS	79, 83, 87, 89, 92	GND	Analog Ground.
PVDD	97	PWR	PLL Analog VDD, 3.3V
PVSS	98	GND	PLL Analog Ground.

2.4 HDCP Keys

The EP169 uses an external 8K-bit EEPROM (24C08) to store the encrypted HDCP keys and BKSV. The page 0/1 (the lower 512 bytes) of the EEPROM is reserved for end user to use. The encrypted HDCP device keys and BKSV are put in page 2/3 (the higher 512 bytes, starting address 0x200) of the EEPROM.

In order to maintain the confidentiality of the HDCP keys which required by the HDCP specification, the 40 56-bit words HDCP keys and the 40-bit BKSV are encrypted before programmed into the EEPROM. The proprietary software licensed from Explore Microelectronics encrypts the HDCP keys and creates formatted EEPROM images for use. The EP169 includes hardware for decrypting the formatted keys in the external EEPROM. The royalty free encryption software will be provided only after customers provide evidence of a complete HDCP Adopter License Agreement and sign Explore's software license agreement. The Adopter License Agreement is maintained by Digital Content Protection, LLC, and can be downloaded from www.digital-cp.com. To obtain Explore Software License Agreement, contact the sales representative of the Explore Microelectronics.

2.5 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	-0.3		4.0	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O	Output Voltage	-0.3		V_{cc} + 0.3	V
T_J	Junction Temperature	-25		125	°C
T_{STG}	Storage Temperature	-65		150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient)		49		°C/W

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Supply Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified**)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
V_{CINL}	Input Clamp Voltage[1]	I_{CL} = -18mA			GND - 0.8	V
V_{CIPL}	Input Clamp Voltage[1]	I_{CL} = 18mA			IVCC + 0.8	V
V_{CONL}	Output Clamp Voltage[1]	I_{CL} = -18mA			GND - 0.8	V
V_{COPL}	Output Clamp Voltage[1]	I_{CL} = 18mA			OVCC + 0.8	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

NOTES:

1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3ns or one third of the clock cycle.

DC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OHD}	Output High Drive Data and Controls	V_{OUT} = 1.2V	7.0	12.0		mA
I_{OLD}	Output Low Drive Data and Controls	V_{OUT} = 0.8V	-7.0	-12.0		mA
V_{ID}	Differential Input Voltage, Single Ended Amplitude		75		1000	mV
I_{PD}	Power-Down Current	PWR_UP = LOW No RXC+/- input		7		mA
I_{CCR}	Receiver Supply Current	DCLK=82.5MHz, 2-pixel/clock mode C_{LOAD} = 10pF R_{EXT_SWING} = 510 ohm Typical Pattern[1]		239		mA
		Worst Case Pattern[2]		358		mA

NOTES:

1. The typical Pattern contains a gray scale area, checkerboard area and text
2. Black and white checkerboard pattern, each checker is two pixels wide.

AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew[1]	165 MHz			245	ps
T_{CCS}	Channel to Channel Differential Input Skew[1]	165 MHz			4	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter Tolerance[2,3]	65 MHz			465	ps
		112 MHz			270	ps
		165 MHz			182	ps
D_{LHT}	Low-to-High Transition Time: DCLK, Data and Controls (70°C, 165MHz)	C_L = 10pF			2.4	ns
D_{HLT}	High-to-Low Transition Time: DCLK, Data and Controls (70°C, 165MHz)	C_L = 10pF			2.3	ns
T_{SETUP}	Data, DE, VSYNC, HSYNC and CTL[3:0] Setup Time to DCLK active edge at 165MHz	C_L = 10pF	1.0			ns
T_{HOLD}	Data, DE, VSYNC, HSYNC and CTL[3:0] Hold Time from DCLK active edge	C_L = 10pF	1.5			ns
T_{CIP}	DCLK Cycle Time		6.06		40	ns

F_{CIP}	DCLK Frequency		25		165	MHz
T_{CIH}	DCLK High Time[4]	C_L = 10pF	1.7			ns
T_{CIL}	DCLK Low Time[4]	C_L = 10pF	2.0			ns
T_{PDL}	Delay from OUT_EN Low to High Impedance outputs				10	ns
T_{LINK_OFF}	Link Disabled (Tx power down) to LINK_ON Low[5]				10	ms
T_{LINK_ON}	Link Enabled (Clock Present) to LINK_ON High				10	ms

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronical Measurement Procedures*
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5. Measured when transmitter was powered down and no TMDS clock presented.

2.6 Timing Diagrams

Figure 2-3 Digital Output Transition Timing Definition

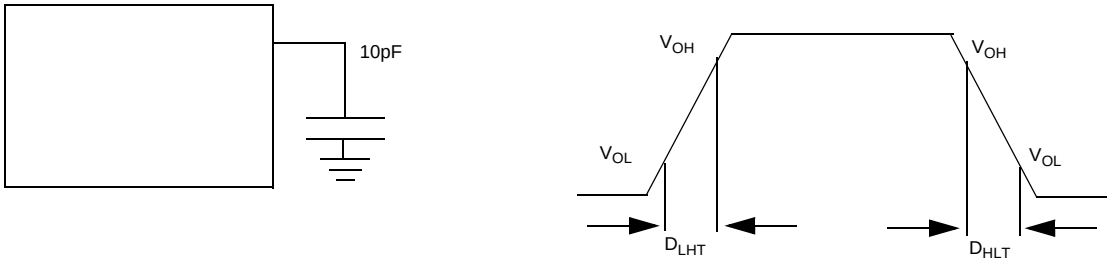


Figure 2-4 Clock Cycle and High/Low Timing Definition

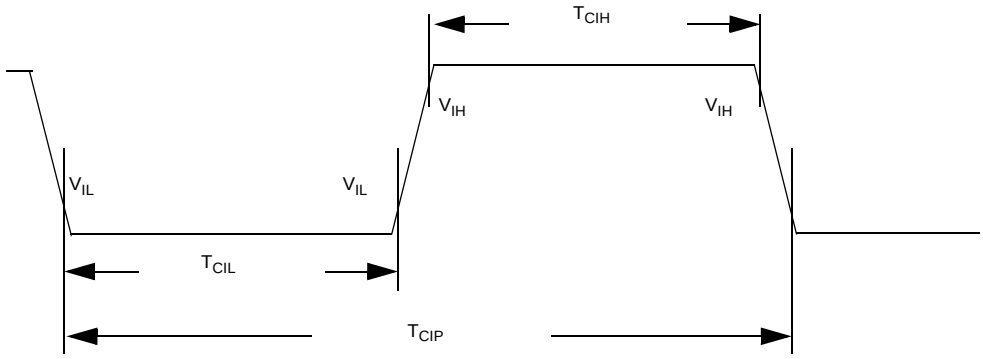


Figure 2-5 Channel to Channel Skew Timing Definition

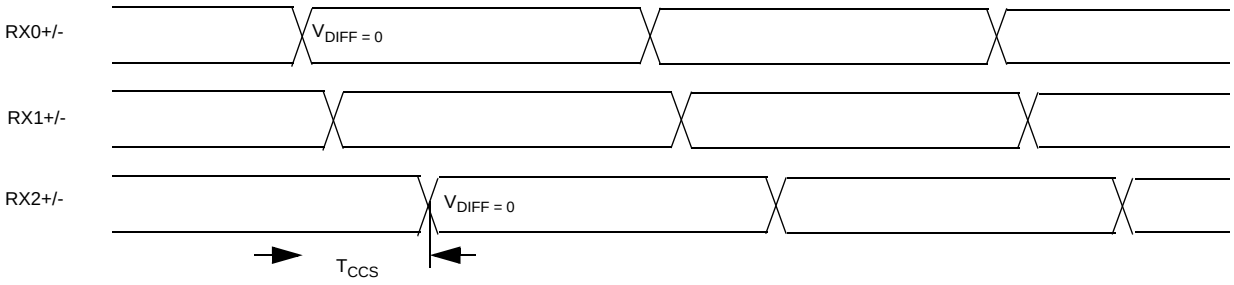


Figure 2-6 Output to DCLK Timing Definition

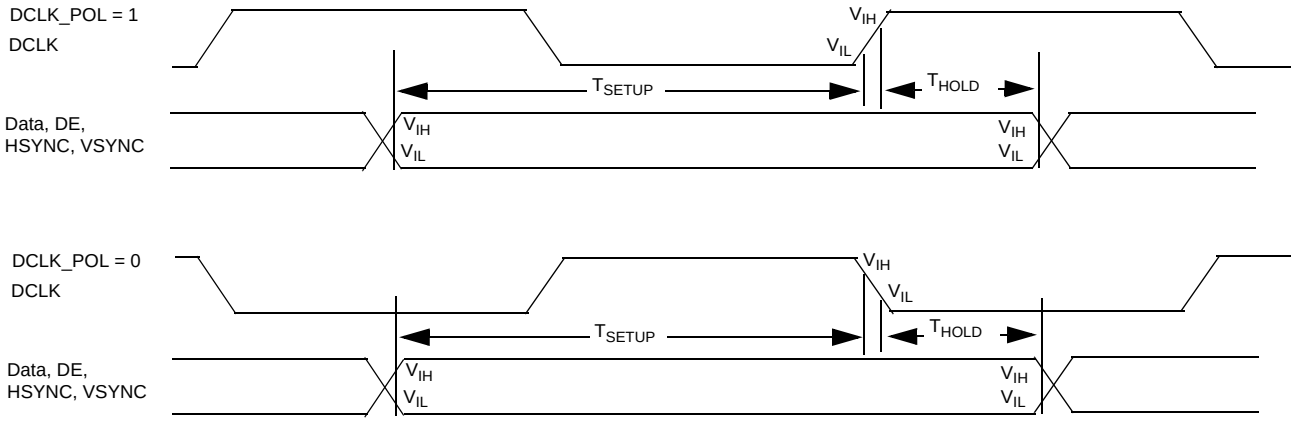


Figure 2-7 LINK_ON Output Timing Definition

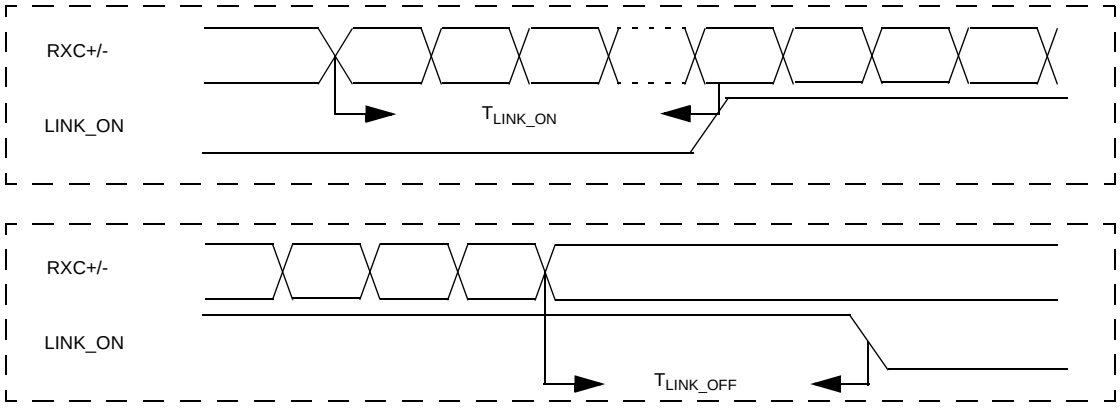
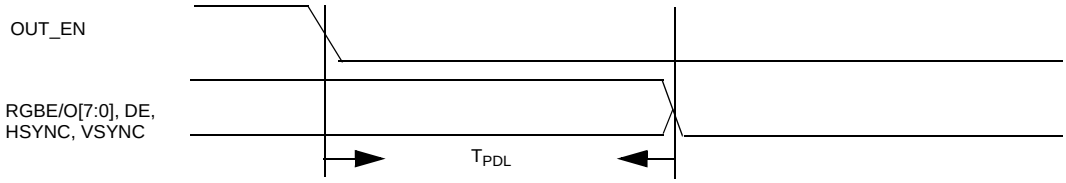
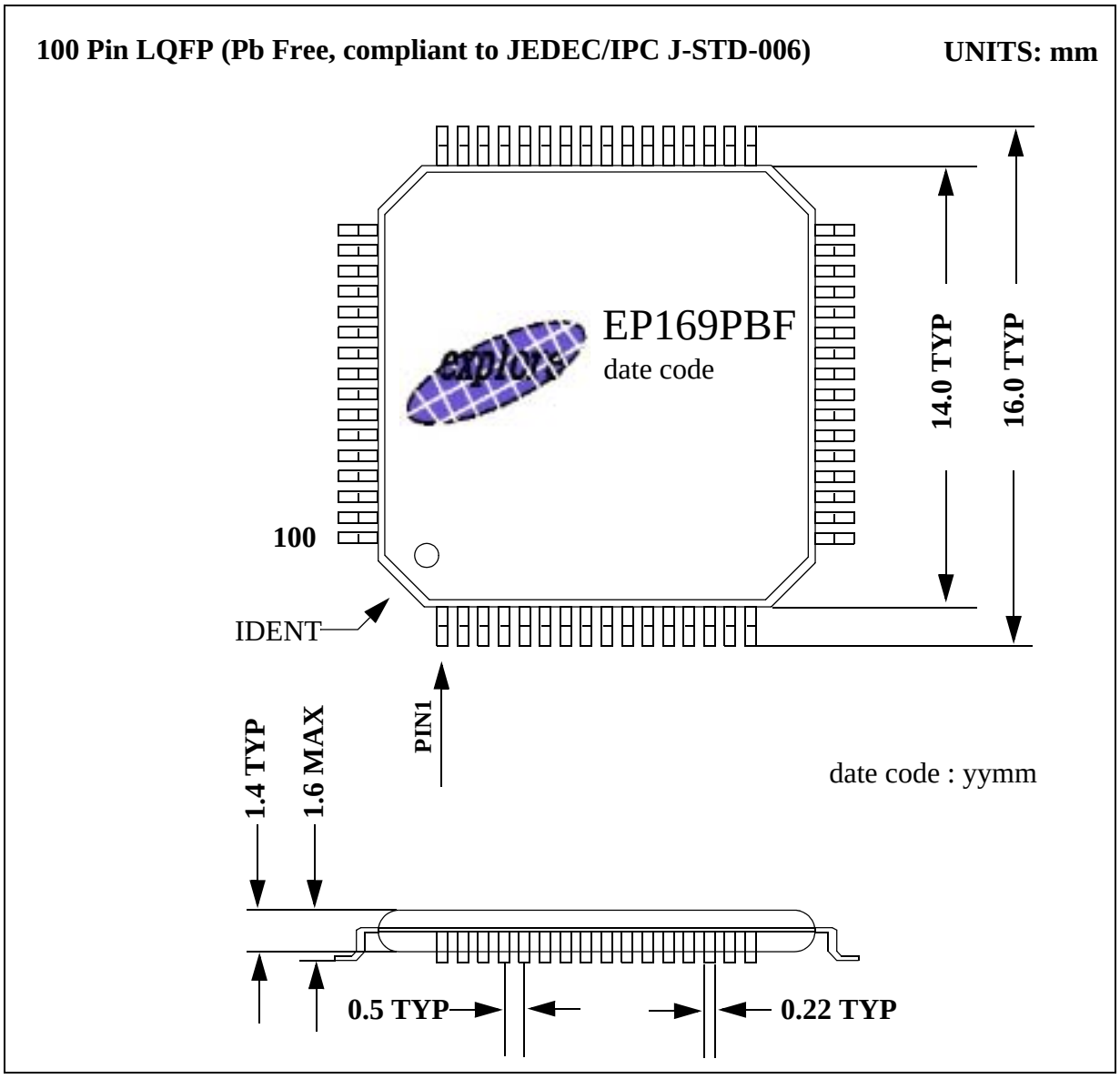


Figure 2-8 OUT_EN to Output Signals Disabled Timing Definition



2.7 Package

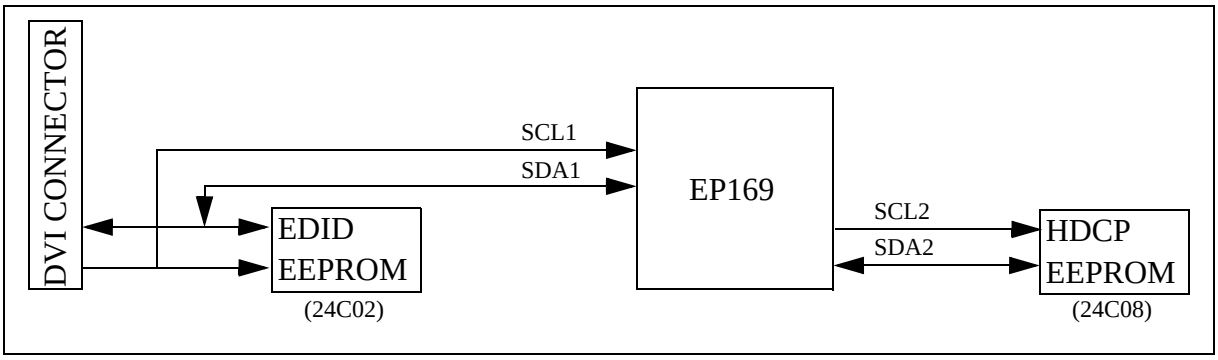

100 Pin LQFP (Pb Free, compliant to JEDEC/IPC J-STD-006)
UNITS: mm
EP169PBF
date code
14.0 TYP
16.0 TYP
100
IDENT
PIN1
1.4 TYP
1.6 MAX
date code : yymm
0.5 TYP
0.22 TYP

Appendix A EEPROM and HDCP Contents

A.1 EEPROM Application

The following application block diagram shows the system configuration of the EP169

Figure A-1 Application Block Diagram of EP169



A.2 HDCP Memory Mapping and Encoding Algorithm

Explore Microelectronics will provide an application program to convert the raw HDCP secret keys to the encrypted keys. Please contact sales representative for more details.

User Guide End Sheet

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