

DVI Compliant Receiver EP161A

User Guide V0.3

Revised: Jun. 29, 2007

Original Release Date: Nov. 11, 2002

Explore Microelectronics, Taiwan

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Revision History

Version Number	Revision Date	Author	Description of Changes
0.1	Nov/11/2002	--	Initial Version
0.2	Mar/24/2005	Ether Lai	Align with EP161 User Guide V0.6
0.2a	Aug/31/2005	Ether Lai	Fix Package Typo
0.3	Jun/29/2007	Ether Lai	Add Electrical Characteristics Notes

Section 1 Introduction

1.1 Overview

The EP161A is a low cost DVI receiver in 100-pin LQFP package. It is compliant to DVI Revision 1.0 specification and supports display resolution from VGA to SXGA (25 - 135MHz) in 1 or 2 pixels/clock mode. The build-in PLL requires no external component. The on-chip Link On detection circuit works even when the chip is put in Power Down mode.

1.2 Features

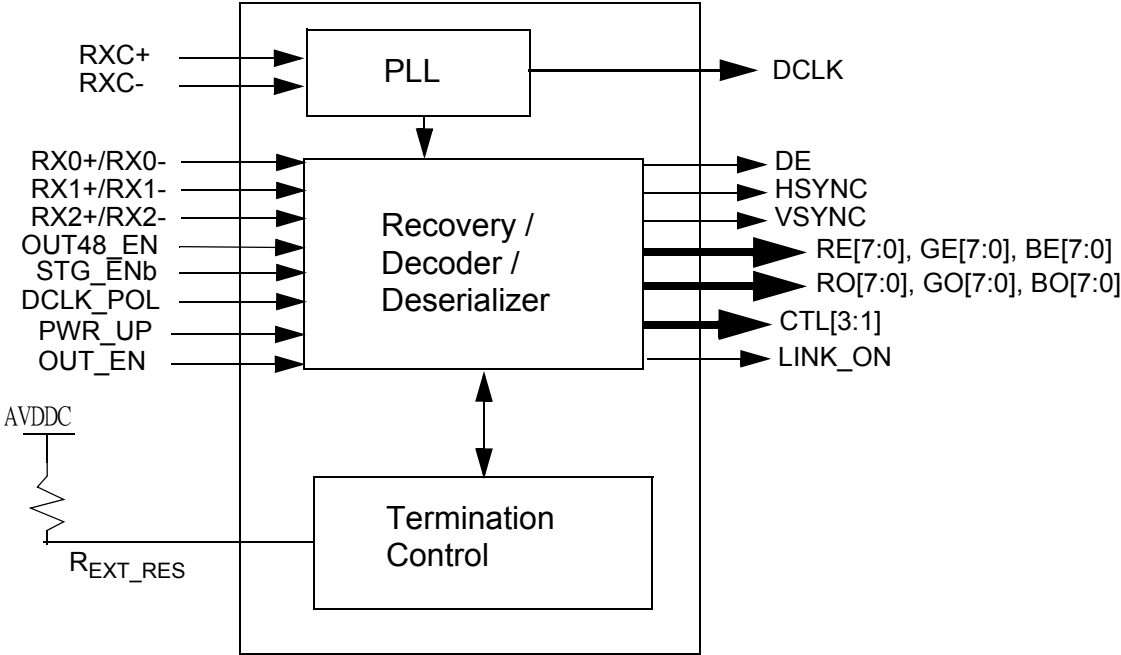
The DVI Receiver EP161A includes these distinctive features:

- DVI specification 1.0 compliant
- Operation pixel frequency range: 25MHz - 135MHz
- PLL requires no external components
- High skew tolerance: 1 full input clock cycle
- Low current consumption in Power Down mode
- Link On detection even in Power Down mode
- Controllable tri-state for output port
- Single 3.3V CMOS design
- 100-pin LQFP (Pb free, compliant to JEDEC/IPC J-STD-006)
- Pin Compatible with Silicon Image SiI161B

Section 2 Overview

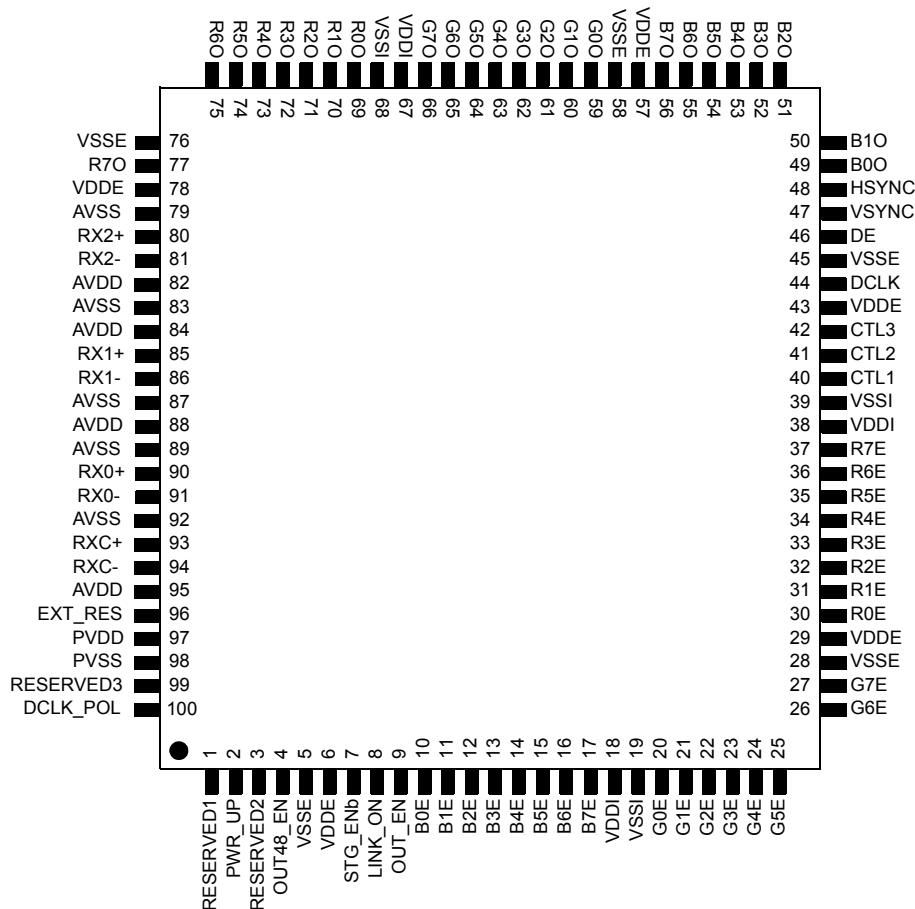
2.1 Block Diagram

Figure 2-1 Block Diagram of DVI Receiver EP161A



2.2 Pin Diagram

Figure 2-2 Pin Diagram of DVI Receiver EP161A



2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 Output Control/Data/CLK Pins

NAME	PIN #	IN/OUT	DESCRIPTION
R0E~R7E	30~37	OUT	Pixel Even Data Outputs.
G0E~G7E	20~27		When OUT_EN = LOW or PWR_UP = LOW the output drivers are placed
B0E~B7E	10~17		in a high impedance state.

Table 2-1 Output Control/Data/CLK Pins

NAME	PIN #	IN/OUT	DESCRIPTION
R00~R70 G00~G70 B00~B70	69~75, 77 59~66 49~56	OUT	Pixel Odd Data Outputs. When OUT_EN = LOW or PWR_UP = LOW the output drivers are placed in a high impedance state.
DCLK	44	OUT	Data Clock Output. When OUT_EN = LOW or PWR_UP = LOW the output driver is placed in a high impedance state.
DE	46	OUT	Data Enable Output. When OUT_EN = LOW or PWR_UP = LOW the output driver is placed in a high impedance state.
HSYNC	48	OUT	Horizontal Sync Output. When OUT_EN = LOW or PWR_UP = LOW the output driver is placed in a high impedance state.
VSYNC	47	OUT	Vertical Sync Output. When OUT_EN = LOW or PWR_UP = LOW the output driver is placed in a high impedance state.
CTL1	40	OUT	Decoded DVI Control Signal 1 Outputs
CTL2 - CTL3	41~41	OUT	Decoded DVI Control Signal 2 and 3 Outputs. When OUT_EN = LOW or PWR_UP = LOW the output driver is placed in a high impedance state.
LINK_ON	8	OUT	Link On Detect <ul style="list-style-type: none"> • HIGH DVI signals present and the link is active. • LOW DVI signals do not present and the link is off.

Table 2-2 Input Pins

NAME	PIN #	IN/OUT	DESCRIPTION
PWR_UP	2	IN	Power Up. <ul style="list-style-type: none"> • HIGH Normal Operation. • LOW Power Down Mode. All the circuit is powered down except for the Link On detection circuit. DCLK, VSYNC, HSYNC, DE, CTL2/3 and all RGB outputs are put in tri-state.
OUT_EN	9	IN	Output Enable. Pulled up by an internal resistor when left unconnected. <ul style="list-style-type: none"> • HIGH Normal Operation. • LOW Put DCLK, VSYNC, HSYNC, DE, CTL2/3 and all RGB outputs in tri-state.
OUT48_EN	4	IN	Dual Pixel Output Enable. <ul style="list-style-type: none"> • HIGH 2 pixels are output per DCLK using R/G/BxE for 1st pixel and R/G/BxO for 2nd pixel. • LOW 1 pixel is output per DCLK using R/G/BxE.

Table 2-2 Input Pins

NAME	PIN #	IN/OUT	DESCRIPTION
STG_ENb	7	IN	Staggered Output Enable. Active low. <ul style="list-style-type: none"> HIGH Selects normal simultaneous outputs on all even and odd data lines. LOW Selects Staggered output drive by delaying even data lines by 1/4 DCLK cycle. This function is only available when OUT48_EN = HIGH.
DCLK_POL	100	IN	Data Clock Polarity. <ul style="list-style-type: none"> HIGH Outputs are triggered by falling edge of DCLK. LOW Outputs are triggered by rising edge of DCLK.

Table 2-3 Reserved Pin

NAME	PIN #	IN/OUT	DESCRIPTION
RESERVED1	1	IN	Must be tied LOW or HIGH for normal operation.
RESERVED2	3	IN	Must be tied LOW or HIGH for normal operation.
RESERVED3	99	IN	Must be tied HIGH for normal operation.

Table 2-4 Differential Signal Data Pins

NAME	PIN #	IN/OUT	DESCRIPTION
RX0+ RX0- RX1+ RX1- RX2+ RX2-	90 91 85 86 80 81	Analog	Differential Data Input Pairs. (DVI v1.0 compliant)
RXC+ RXC-	93 94	Analog	Differential Clock Input Pairs. (DVI v1.0 compliant)
EXT_RES	96	Analog	Impedance Matching Control. Resistor value is set ten times the termination resistance of each channel.

Table 2-5 Power and Ground Pins

NAME	PIN #	IN/OUT	DESCRIPTION
VDDI	18, 38, 67	PWR	Internal VDD, 3.3V
VSSI	19, 39, 68	GND	Internal Ground.
VDDE	6, 29, 43, 57, 78	PWR	Pad VDD, 3.3V
VSSE	5, 28, 45, 58, 76	GND	Pad Ground.
AVDD	82, 84, 88 95	PWR	Analog VDD, 3.3V
AVSS	79, 83, 87, 89, 92	GND	Analog Ground.
PVDD	97	PWR	PLL Analog VDD, 3.3V

Table 2-5 Power and Ground Pins

NAME	PIN #	IN/OUT	DESCRIPTION
PVSS	98	GND	PLL Analog Ground.

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{CC}	Supply Voltage	-0.3		4.0	V
V _I	Input Voltage	-0.3		V _{CC} + 0.3	V
V _O	Output Voltage	-0.3		V _{CC} + 0.3	V
T _J	Junction Temperature	-25		125	°C
T _{STG}	Storage Temperature	-65		150	°C
θ _{JA}	Thermal Resistance (Junction to Ambient)		49		°C/W

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V _{CC}	Supply Voltage	3.0	3.3	3.6	V
V _{CCN}	Supply Voltage Noise			100	mV _{p-p}
T _A ¹	Ambient Temperature (with power applied)	0	25	70	°C

NOTES:

1. The EP161A had been proven to work under the following conditions:
 - (a) ambient temperature: -40°C ~ 85°C
 - (b) input pixel clock: 75MHz (1080i or 720p resolution)

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IH}	High-level Input Voltage		2.0			V
V _{IL}	Low-level Input Voltage				0.8	V
V _{OH}	High-level Output Voltage		2.4			V
V _{OL}	Low-level Output Voltage				0.4	V
V _{CINL}	Input Clamp Voltage ¹	I _{CL} = -18mA			GND - 0.8	V
V _{C IPL}	Input Clamp Voltage ¹	I _{CL} = 18mA			IVCC + 0.8	V
V _{CONL}	Output Clamp Voltage ¹	I _{CL} = -18mA			GND - 0.8	V

V_{COPL}	Output Clamp Voltage ¹	$I_{CL} = 18\text{mA}$			$OVCC + 0.8$	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	μA

NOTES:

1. Guaranteed by design. Voltage undershoot or overshoot cannot exceed absolute maximum conditions for a pulse of greater than 3ns or one third of the clock cycle.

DC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OHD}	Output High Drive Data and Controls	$V_{OUT} = 1.2\text{V}$	7.0	12.0		mA
I_{OLD}	Output Low Drive Data and Controls	$V_{OUT} = 0.8\text{V}$	-7.0	-12.0		mA
V_{ID}	Differential Input Voltage, Single Ended Amplitude		75		1000	mV
I_{PD}	Power-Down Current	PWR_UP = LOW No RXC+/- input		5.5	8.0	mA
I_{CCR}	Receiver Supply Current	DCLK=67.5MHz, 2-pixel/clock mode $C_{LOAD} = 10\text{pF}$ $R_{EXT_SWING} = 750\ \text{ohm}$ Typical Pattern ¹		186	222	mA
		Worst Case Pattern ²		288	362	mA

NOTES:

1. The typical Pattern contains a gray scale area, checkerboard area and text
2. Black and white checkerboard pattern, each checker is two pixels wide.

AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew ¹	135 MHz			290	ps
T_{CCS}	Channel to Channel Differential Input Skew ¹	135 MHz			5	ns
T_{IJIT}	Worst Case Differential Input Clock Jitter Tolerance ^{2,3}	65 MHz			465	ps
		112 MHz			270	ps
		135 MHz			220	ps
D_{LHT}	Low-to-High Transition Time: DCLK, Data and Controls (70°C, 135MHz)	$C_L = 10\text{pF}$			2.6	ns
D_{HLT}	High-to-Low Transition Time: DCLK, Data and Controls (70°C, 135MHz)	$C_L = 10\text{pF}$			2.4	ns
T_{SETUP}	Data, DE, VSYNC, HSYNC and CTL[3:0] Setup Time to DCLK active edge at 135MHz	$C_L = 10\text{pF}$	1.0			ns

T _{HOLD}	Data, DE, VSYNC, HSYNC and CTL[3:0] Hold Time from DCLK active edge	C _L = 10pF	1.5			ns
T _{CIP}	DCLK Cycle Time		7.5		40	ns
F _{CIP}	DCLK Frequency		25		135	MHz
T _{CIH}	DCLK High Time ⁴	C _L = 10pF	1.7			ns
T _{CIL}	DCLK Low Time ⁴	C _L = 10pF	2.0			ns
T _{PDL}	Delay from OUT_EN Low to High Impedance outputs				10	ns
T _{LINK_OFF}	Link Disabled (Tx power down) to LINK_ON Low ⁵				10	ms
T _{LINK_ON}	Link Enabled (Clock Present) to LINK_ON High				10	ms

NOTES:

1. Guaranteed by design.
2. Jitter defines as per DVI 1.0 Specification, Section 4.6 *Jitter Specification*.
3. Jitter measured with Clock Recovery Unit as per DVI 1.0 Specification, Section 4.7 *Electronical Measurement Procedures*
4. Output clock duty cycle is independent of the differential input clock duty cycle and the IDCK duty cycle.
5. Measured when transmitter was powered down and no TMDS clock presented.

2.5 Timing Diagrams

Figure 2-3 Digital Output Transition Timing Definition

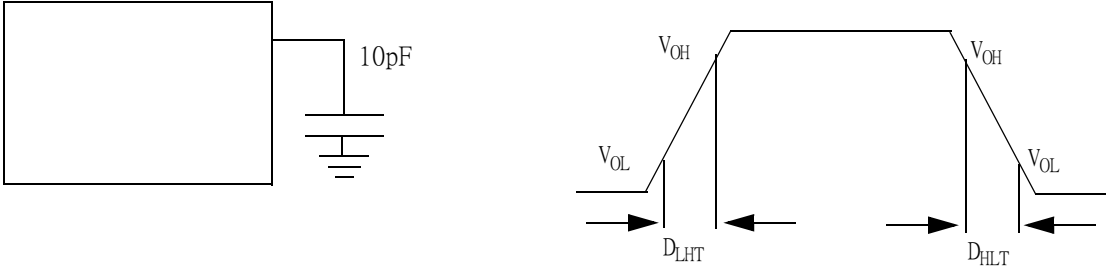


Figure 2-4 Clock Cycle and High/Low Timing Definition

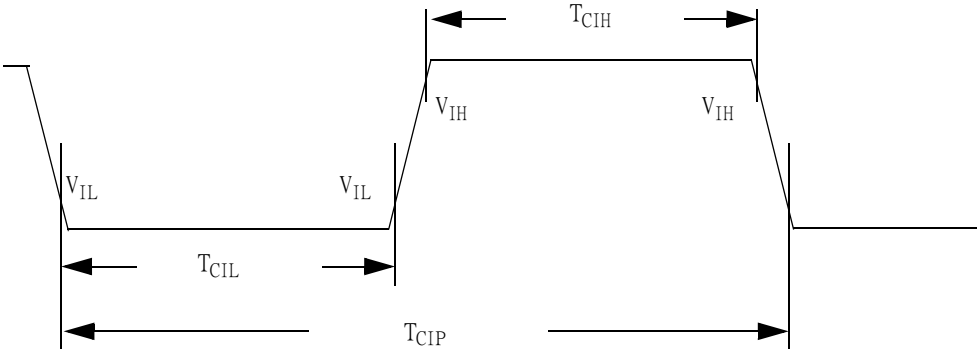


Figure 2-5 Channel to Channel Skew Timing Definition

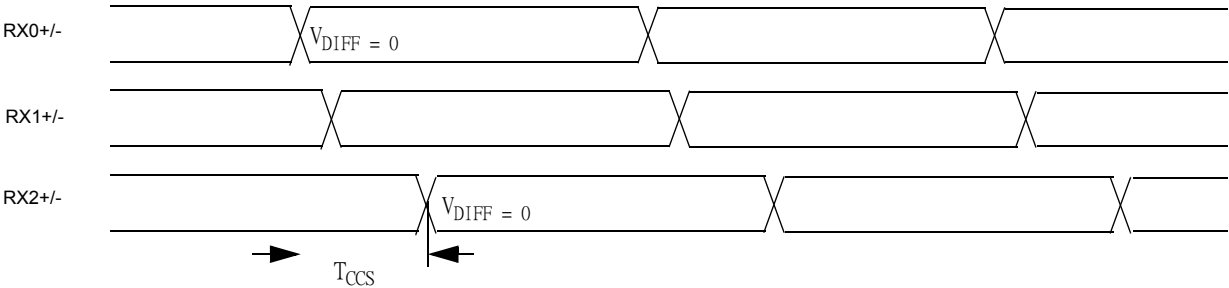


Figure 2-6 Output to DCLK Timing Definition

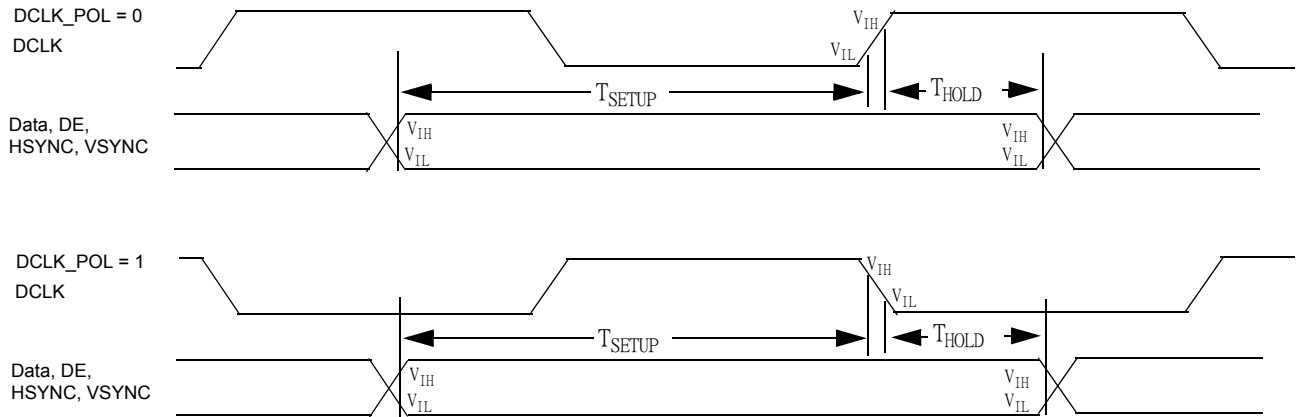


Figure 2-7 LINK_ON Output Timing Definition

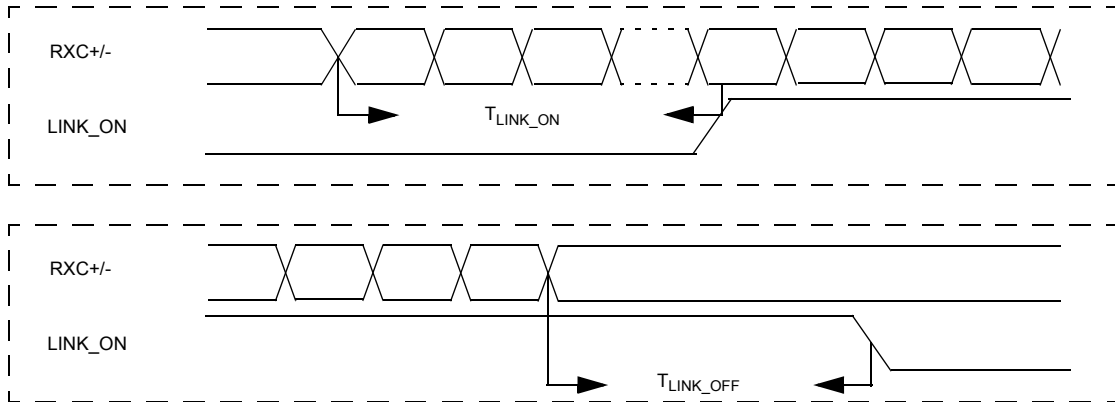
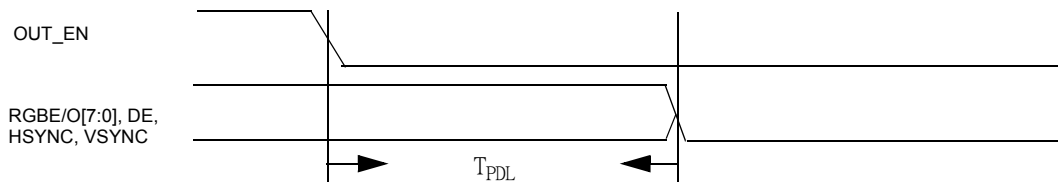
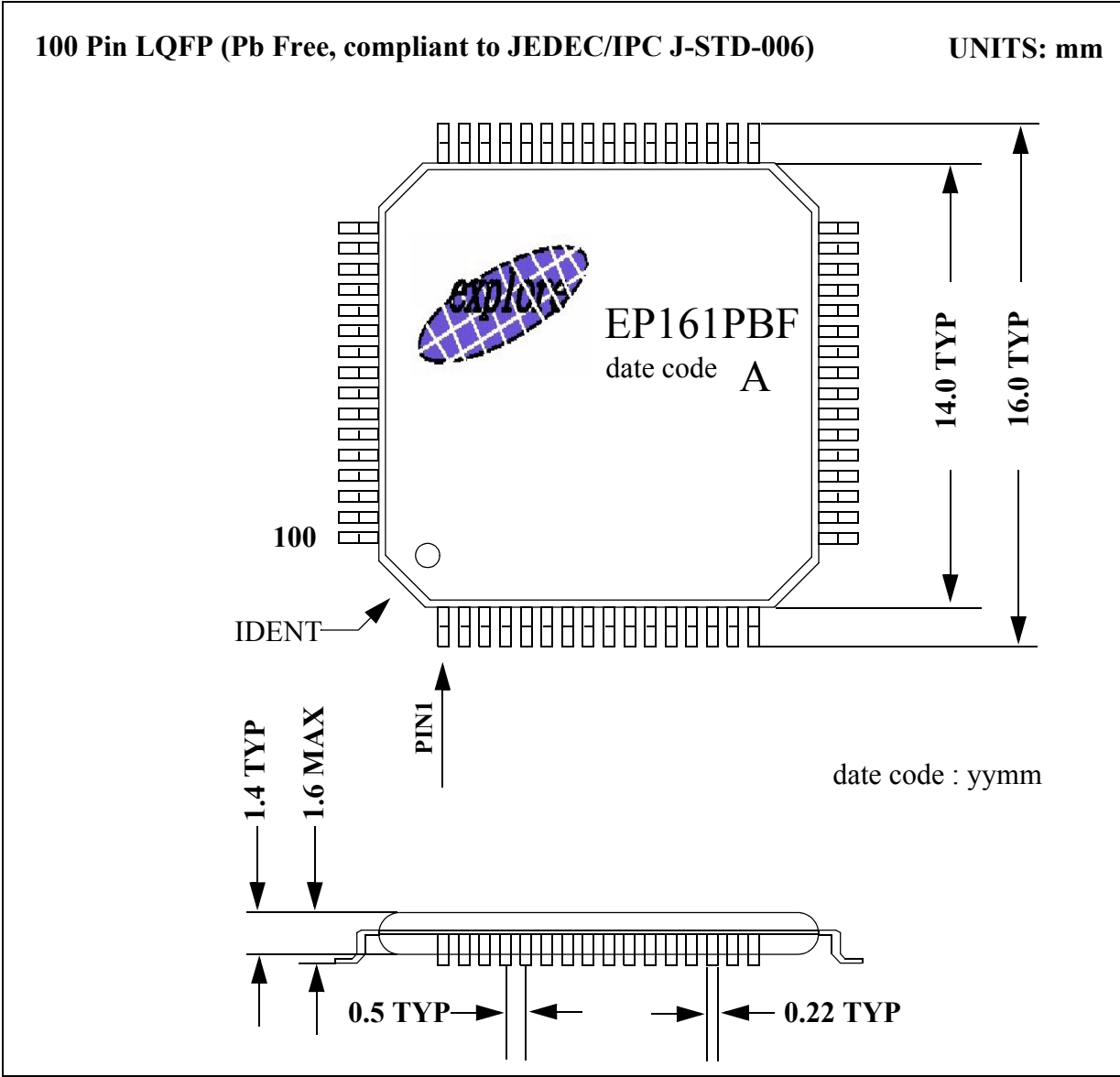


Figure 2-8 OUT_EN to Output Signals Disabled Timing Definition



2.6 Package



User Guide End Sheet

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